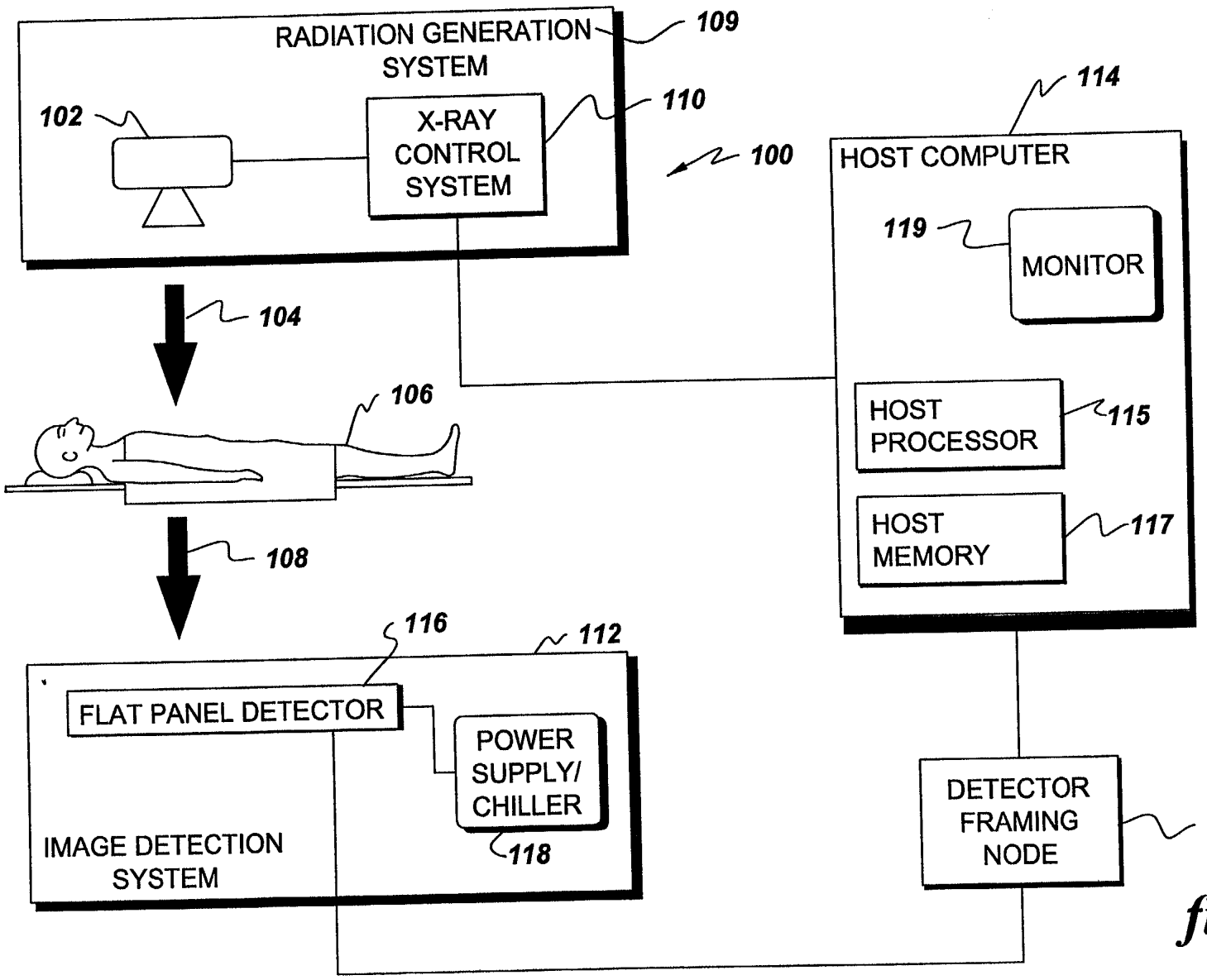

RADIATION GENERATION SYSTEM
109
102
X-RAY CONTROL SYSTEM
110
100
114
HOST COMPUTER
119
MONITOR
104
106
HOST PROCESSOR
115
HOST MEMORY
117
108
116
112
FLAT PANEL DETECTOR
POWER SUPPLY/ CHILLER
118
IMAGE DETECTION SYSTEM
DETECTOR FRAMING NODE
304

fig. 1

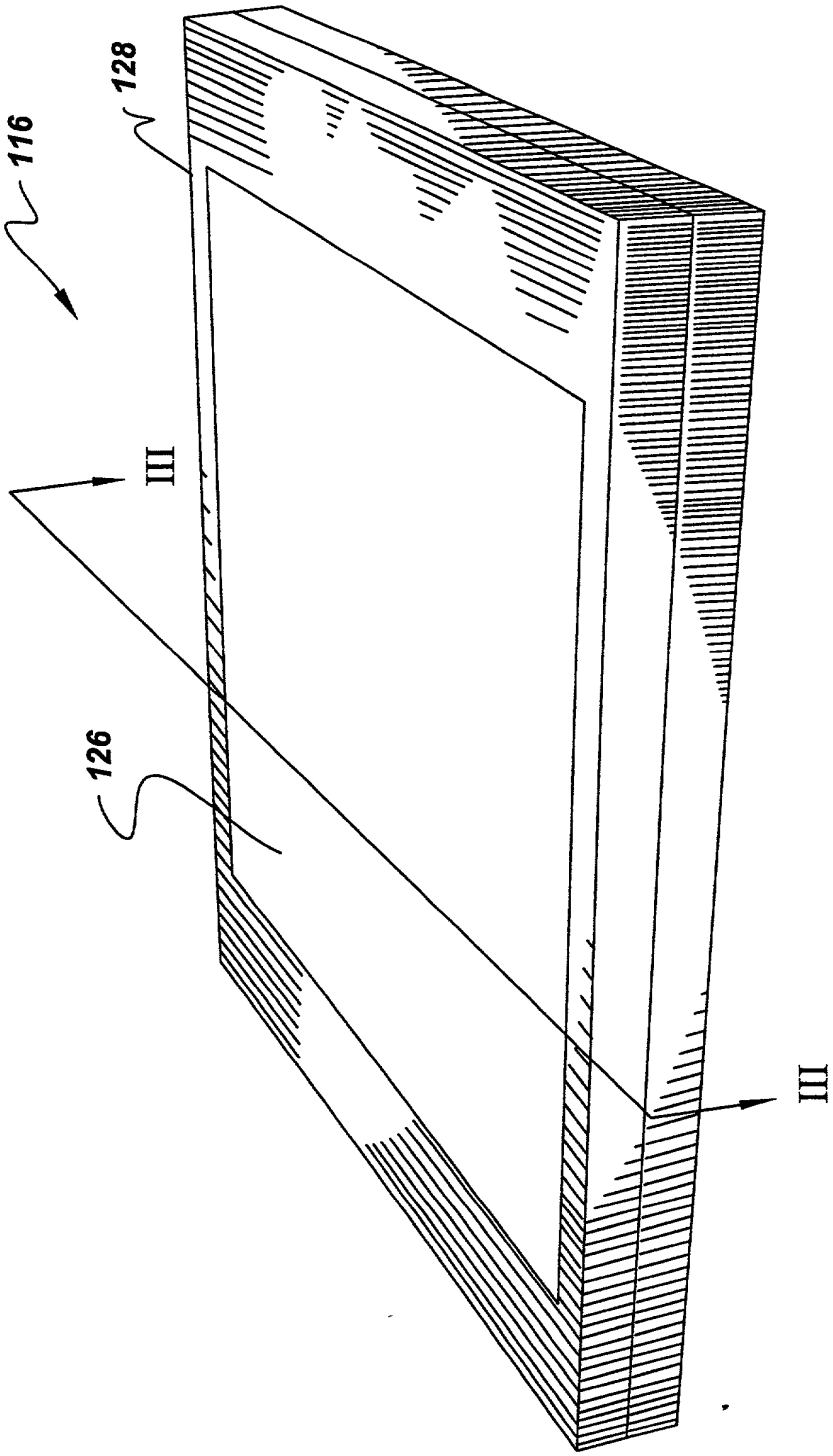


fig. 2
(PRIOR ART)

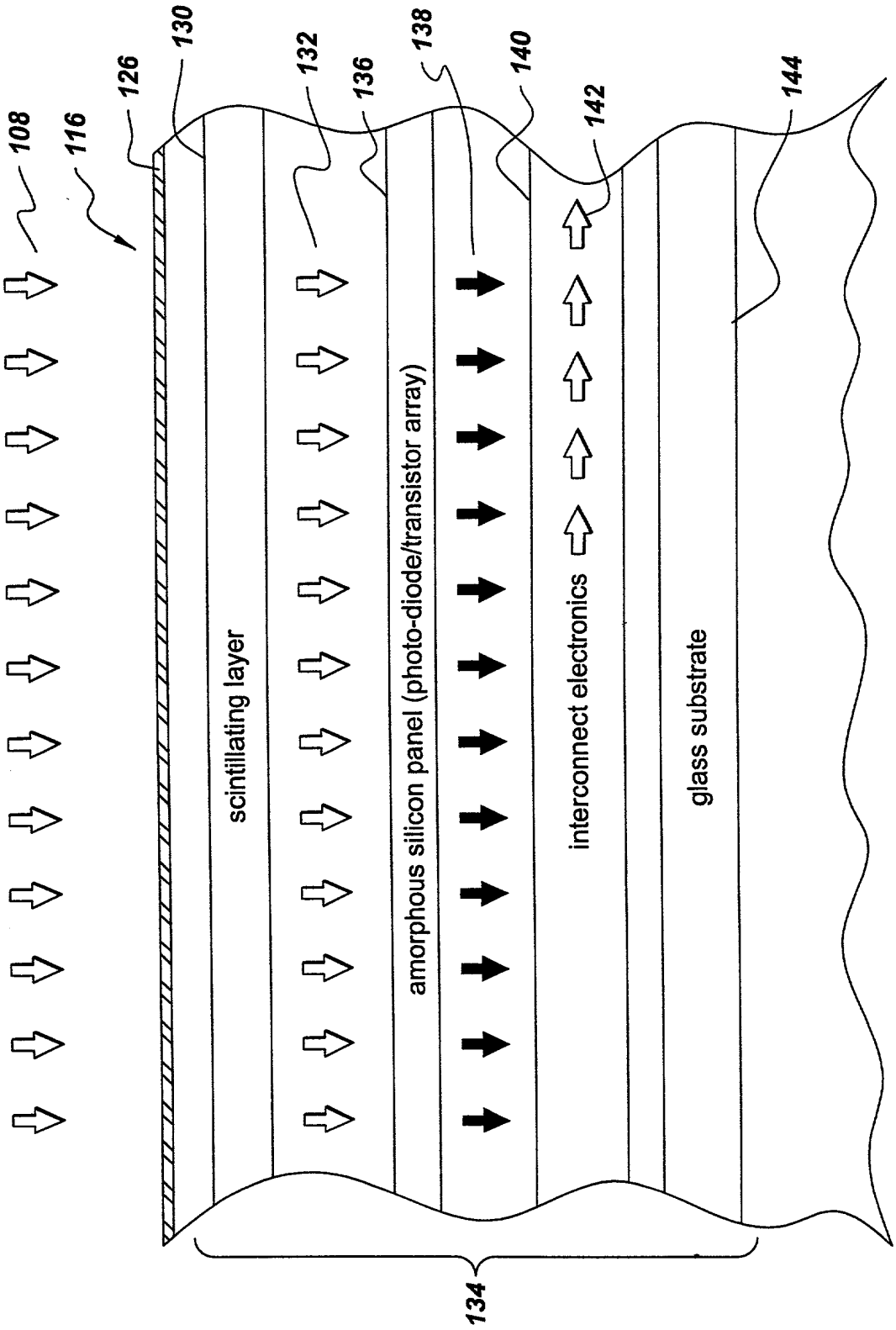

108
116
126
130
132
136
138
140
142
144
scintillating layer
amorphous silicon panel (photo-diode/transistor array)
interconnect electronics
glass substrate
134

fig. 3

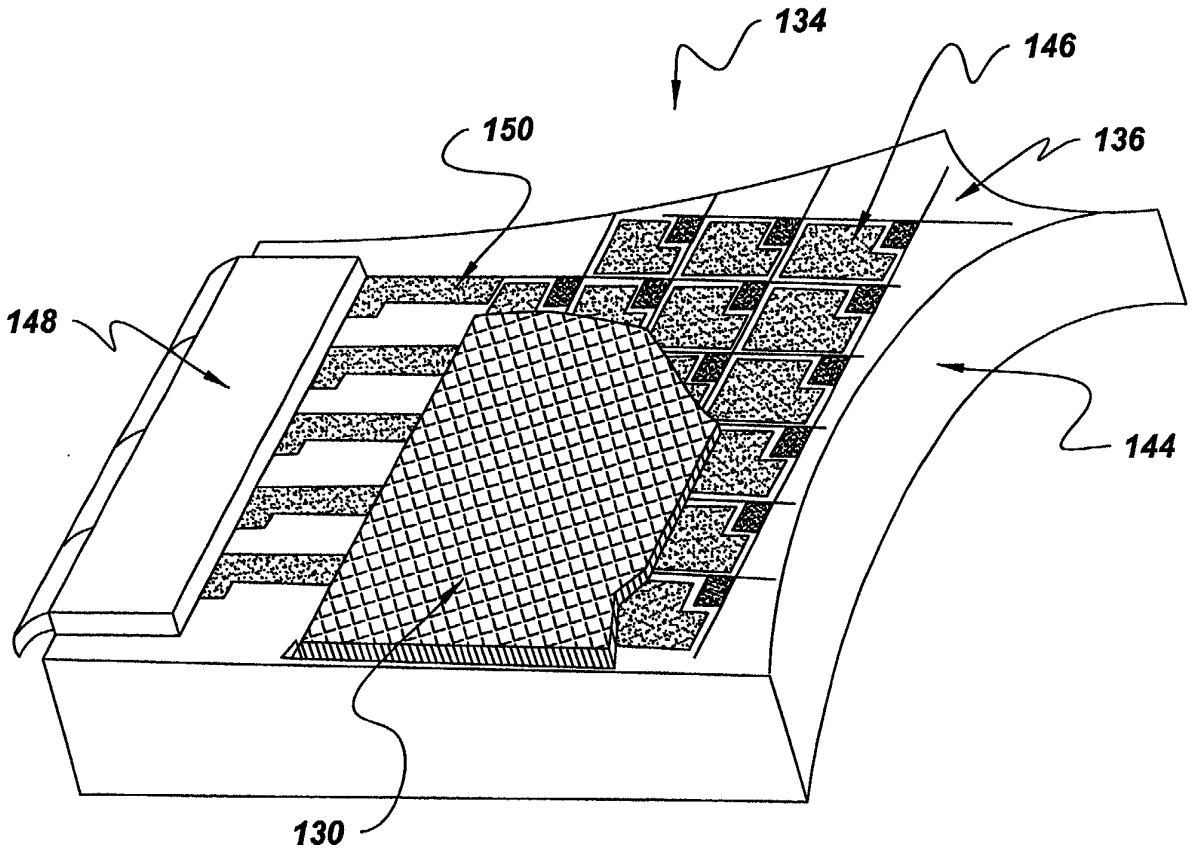


fig. 4
(Prior Art)

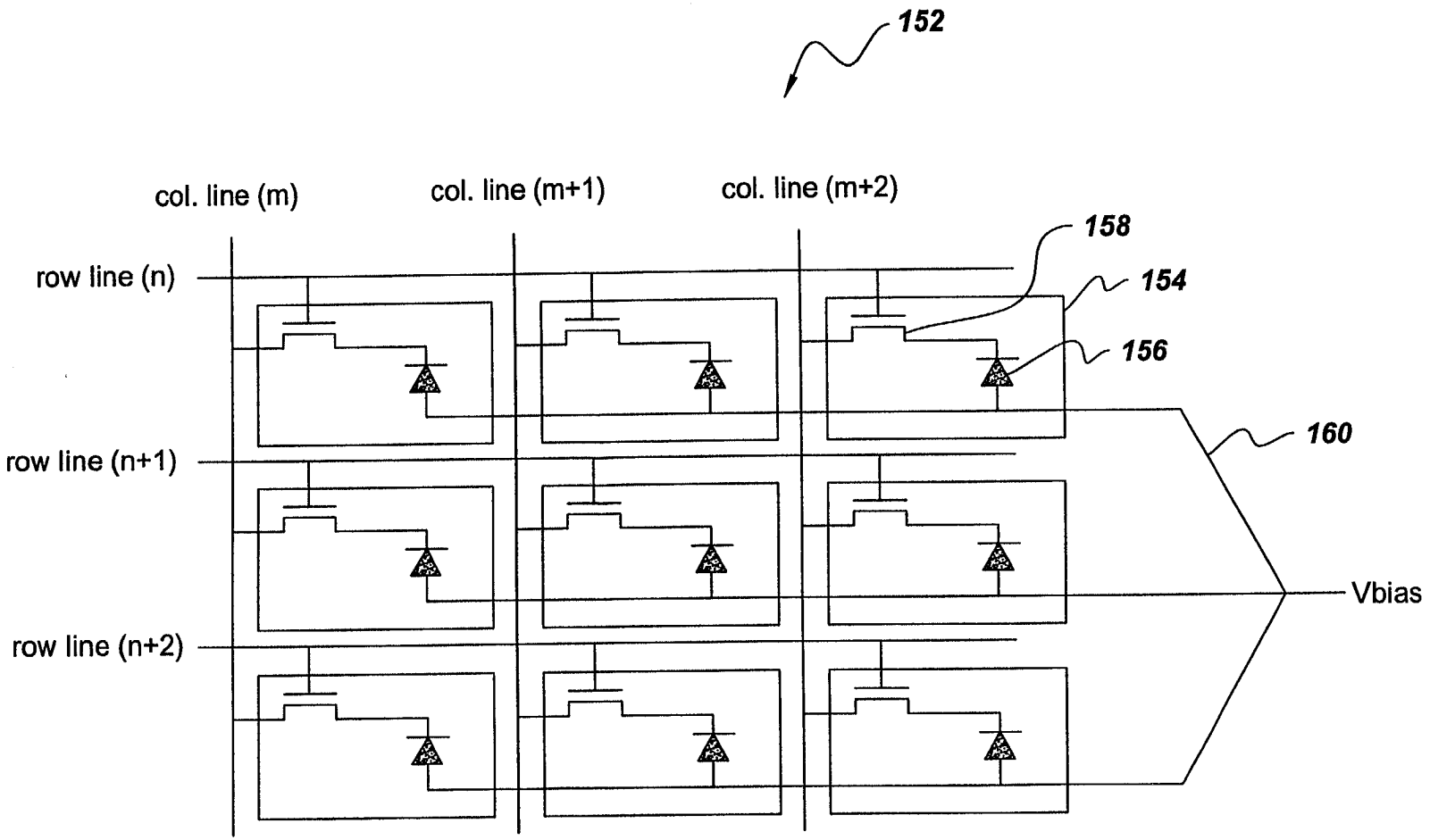


fig. 5
(Prior Art)

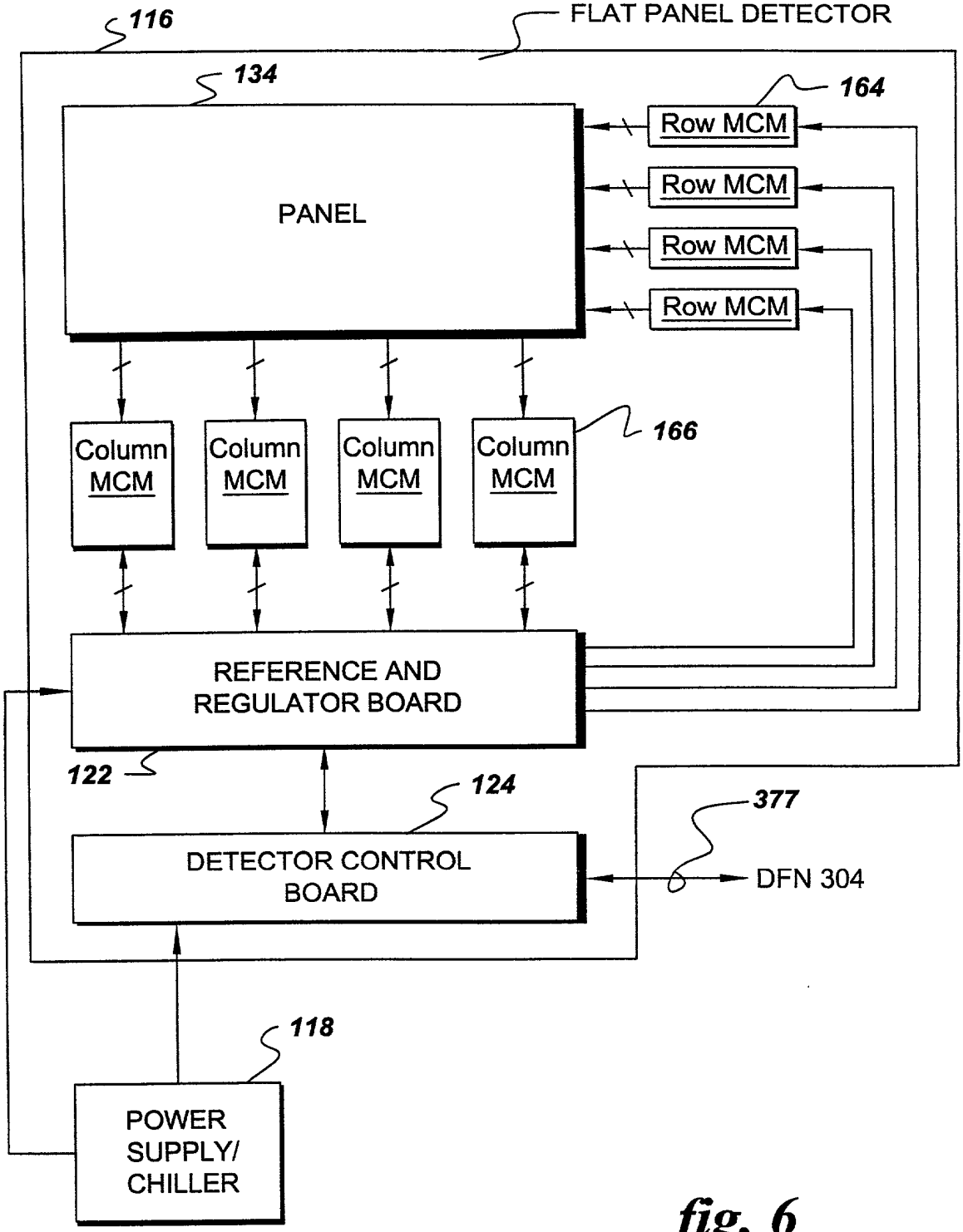


fig. 6
(PRIOR ART)

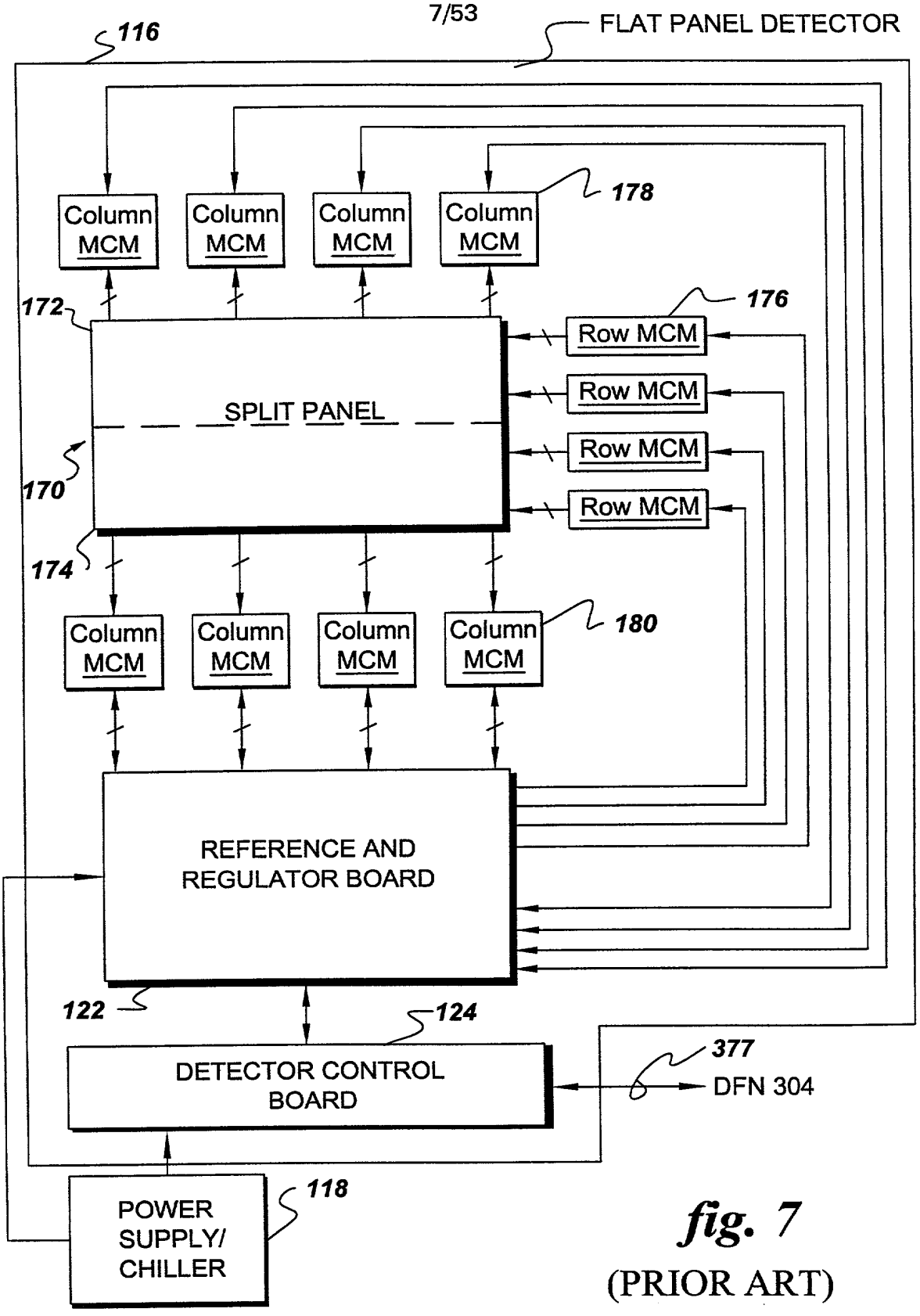


fig. 7
(PRIOR ART)

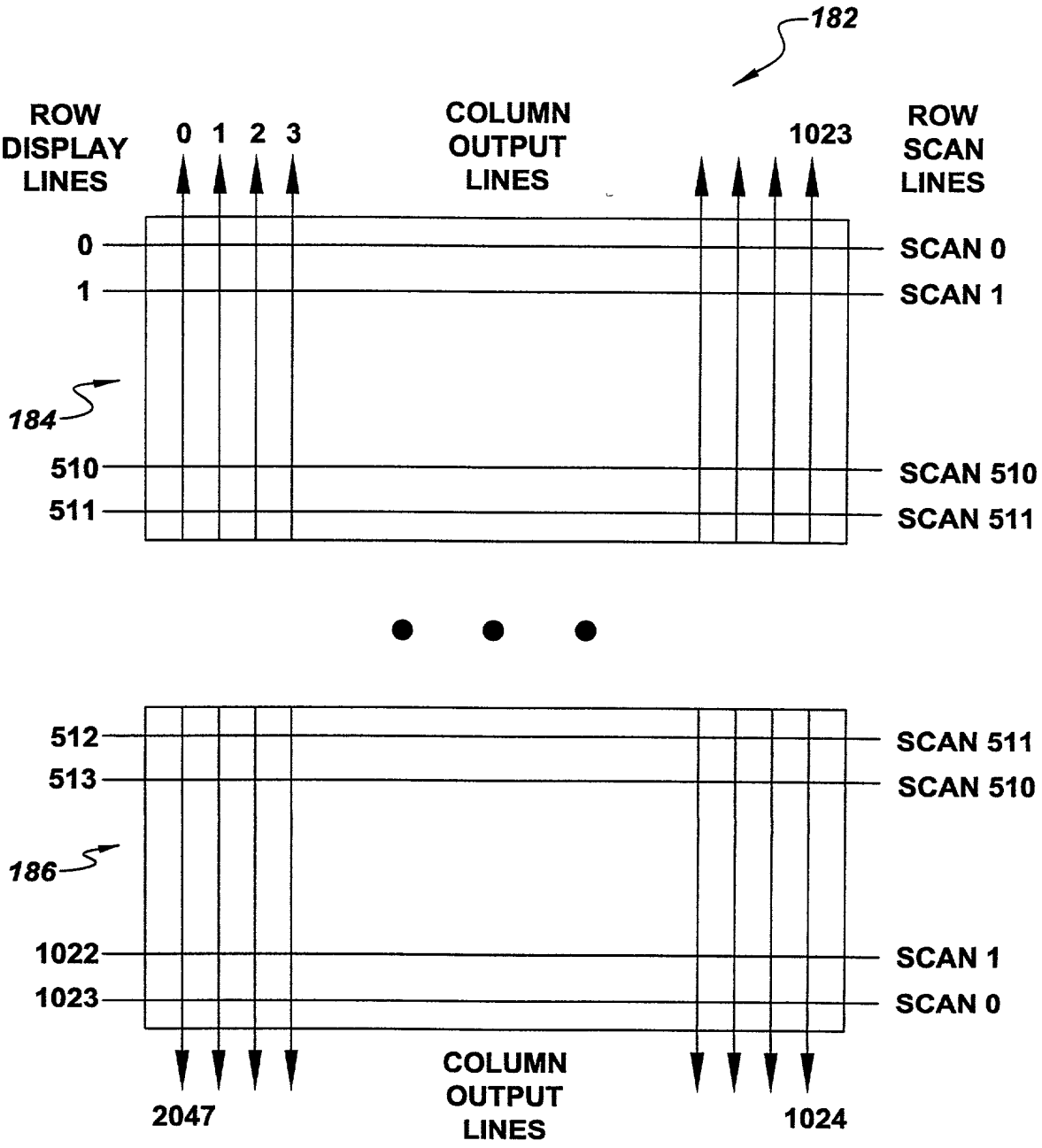


fig. 8
(PRIOR ART)

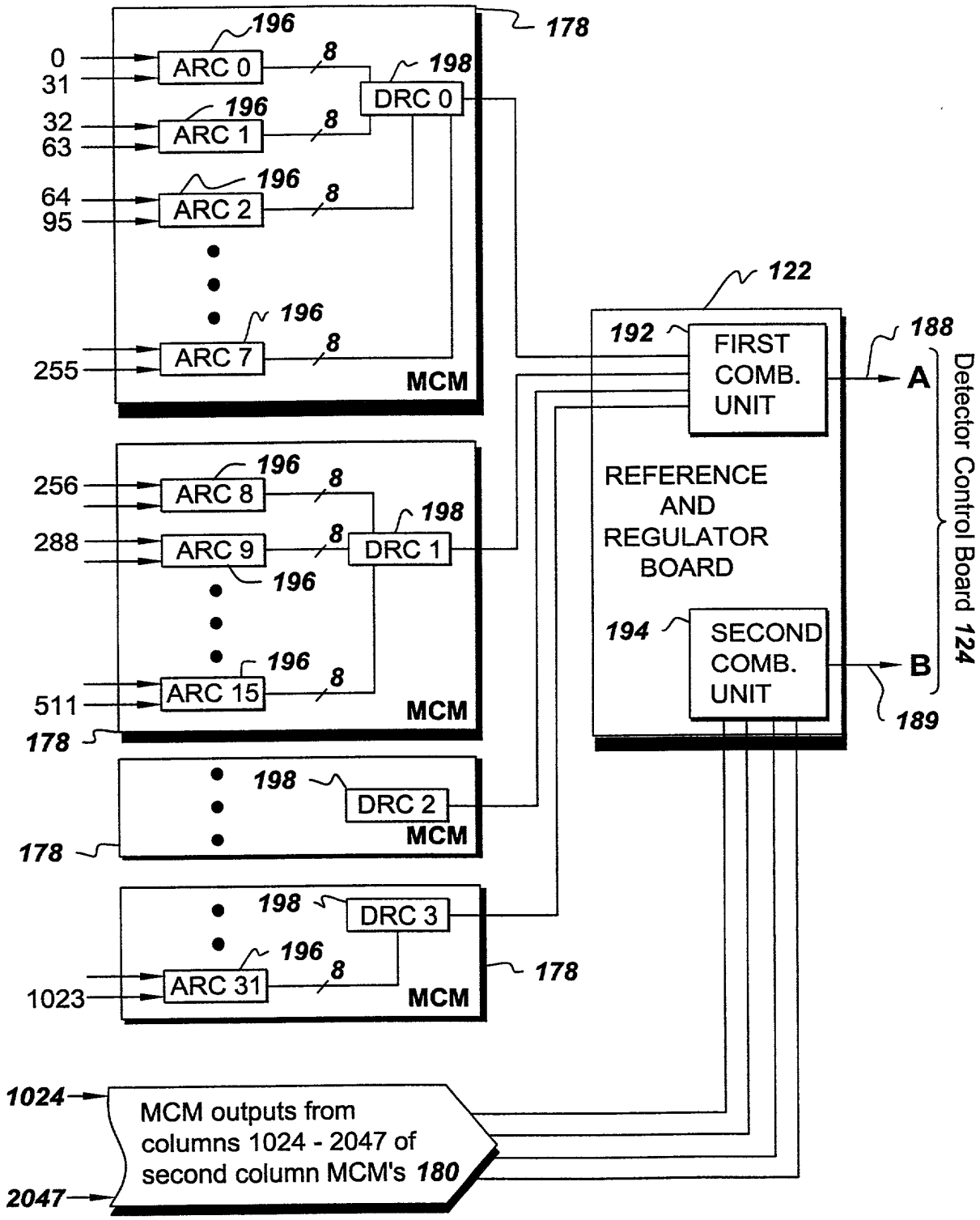


fig. 9 (PRIOR ART)

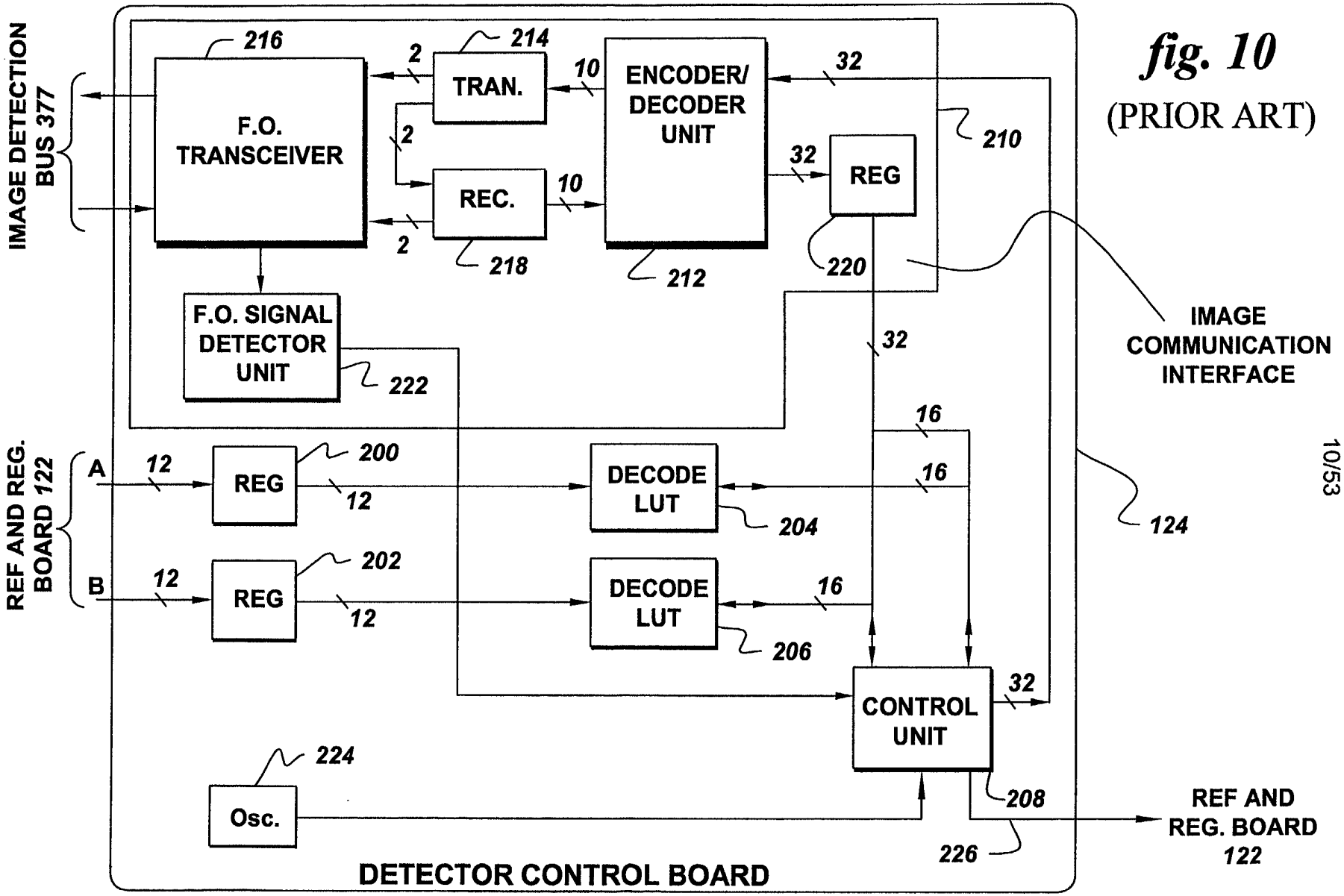
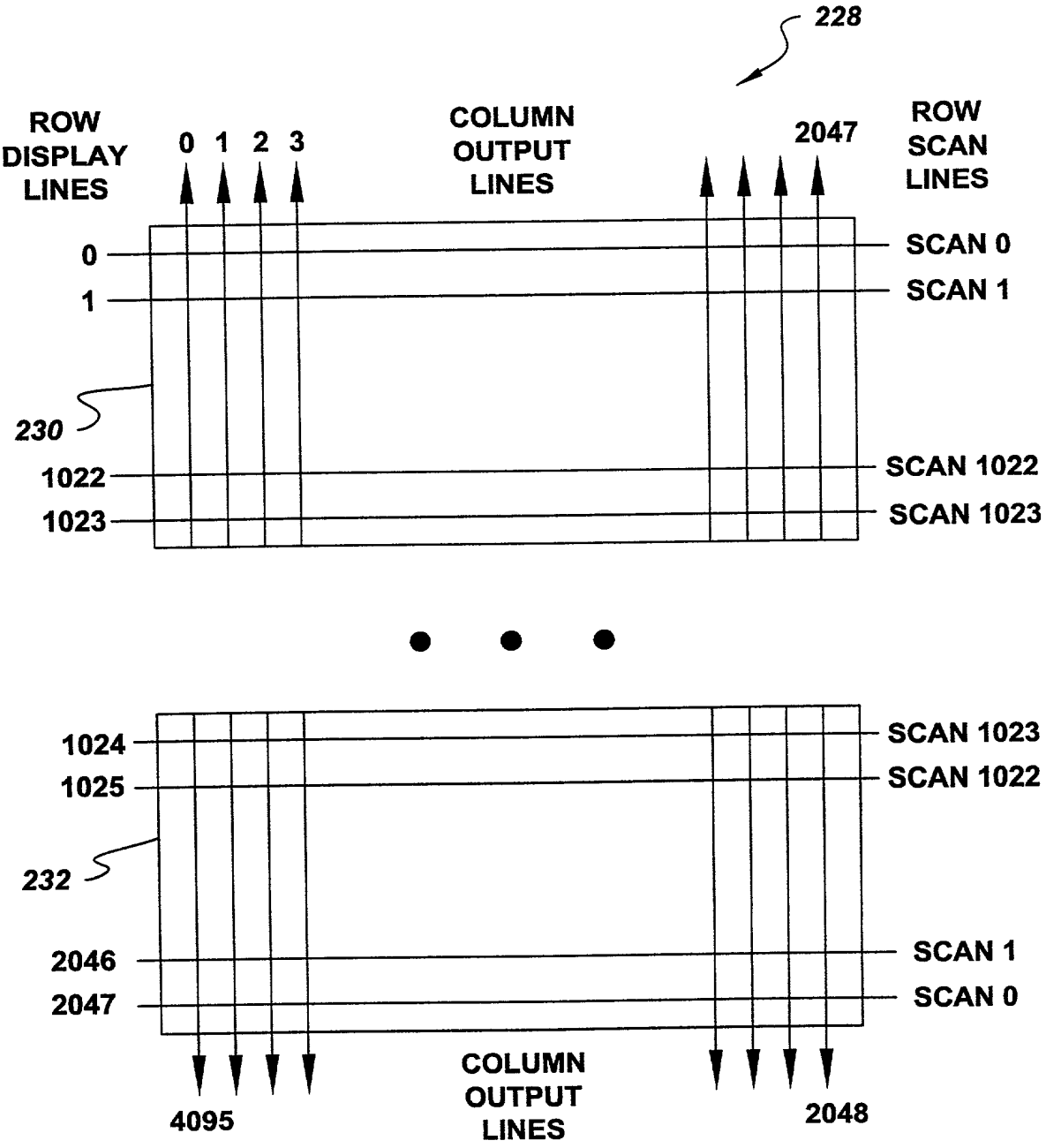


fig. 10
(PRIOR ART)



RADIOGRAPHY DIGITAL X-RAY PANEL

fig. 11 (PRIOR ART)

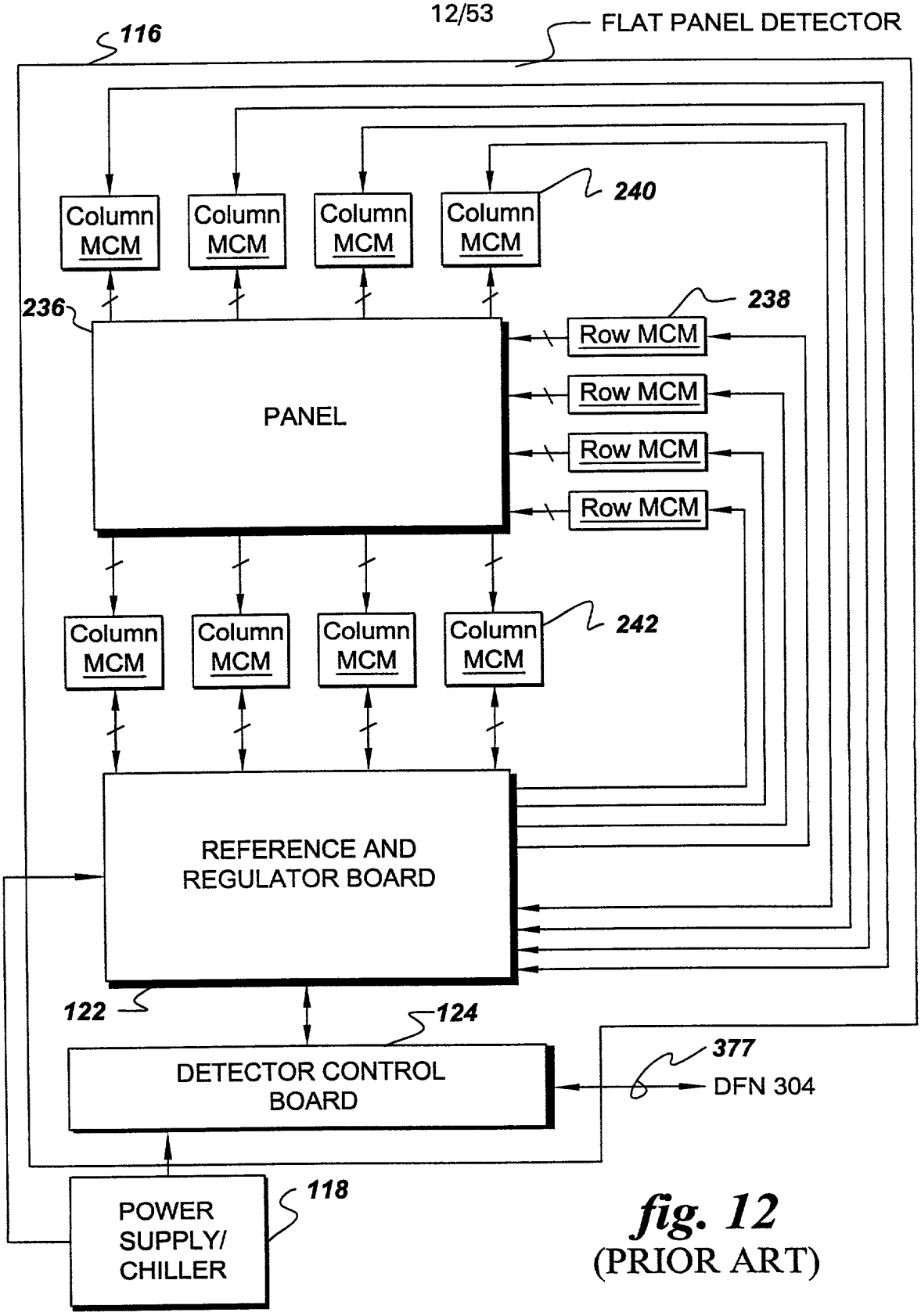
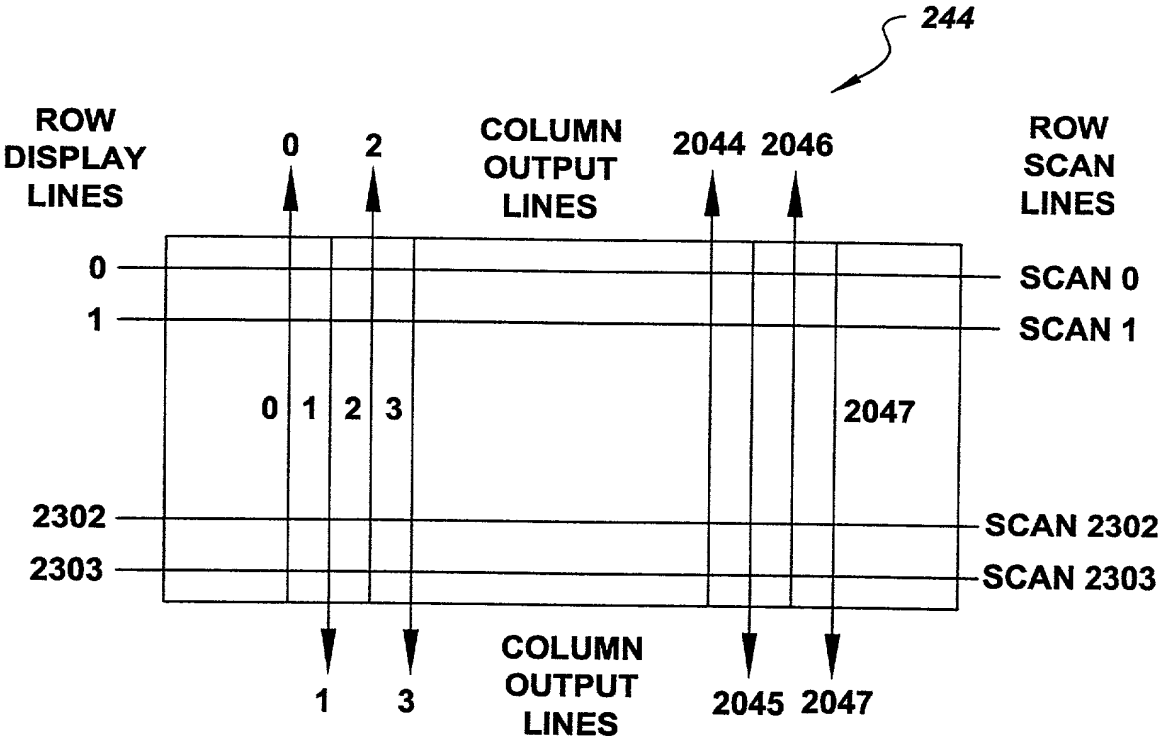


fig. 12
(PRIOR ART)



MAMMOGRAPHY DIGITAL X-RAY PANEL

fig. 13

(PRIOR ART)

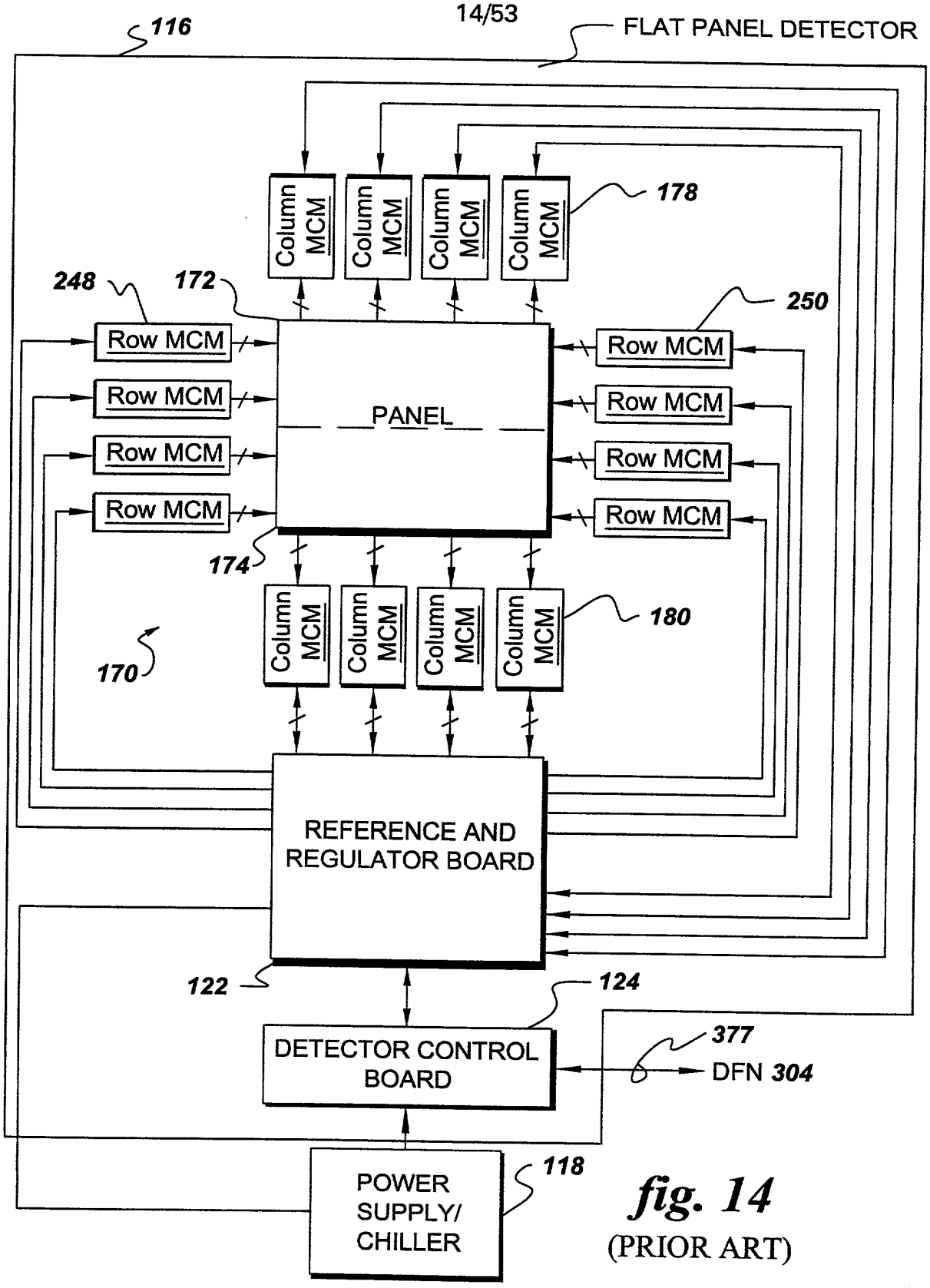


fig. 14
(PRIOR ART)

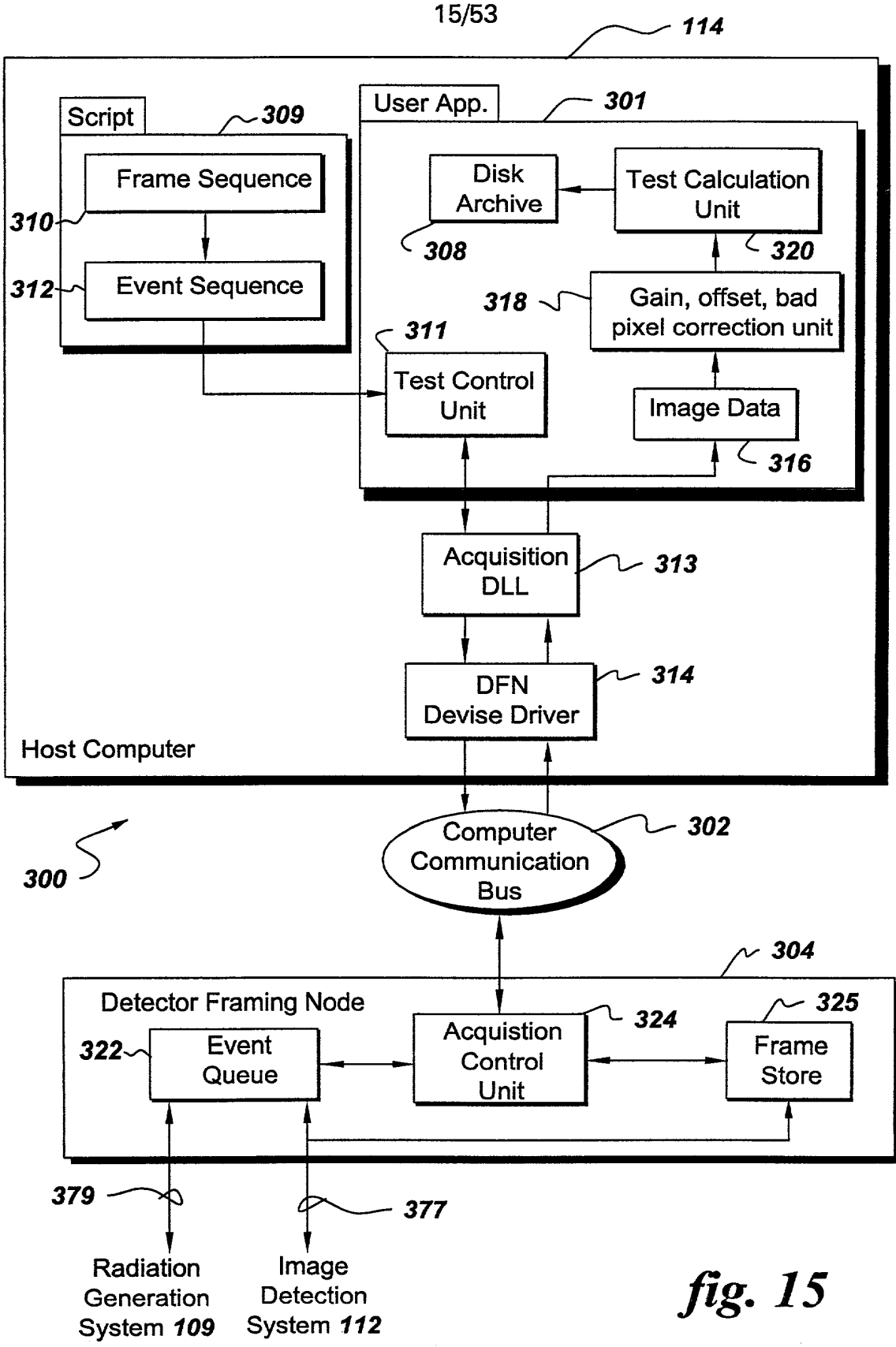

114
Script
309
User App.
301
Frame Sequence
310
Event Sequence
312
Disk Archive
308
Test Calculation Unit
320
318
Gain, offset, bad pixel correction unit
311
Test Control Unit
Image Data
316
Acquisition DLL
313
DFN Devise Driver
314
Host Computer
300
Computer Communication Bus
302
304
Detector Framing Node
322
Event Queue
Acquistion Control Unit
324
325
Frame Store
379
377
Radiation Generation System 109
Image Detection System 112

fig. 15

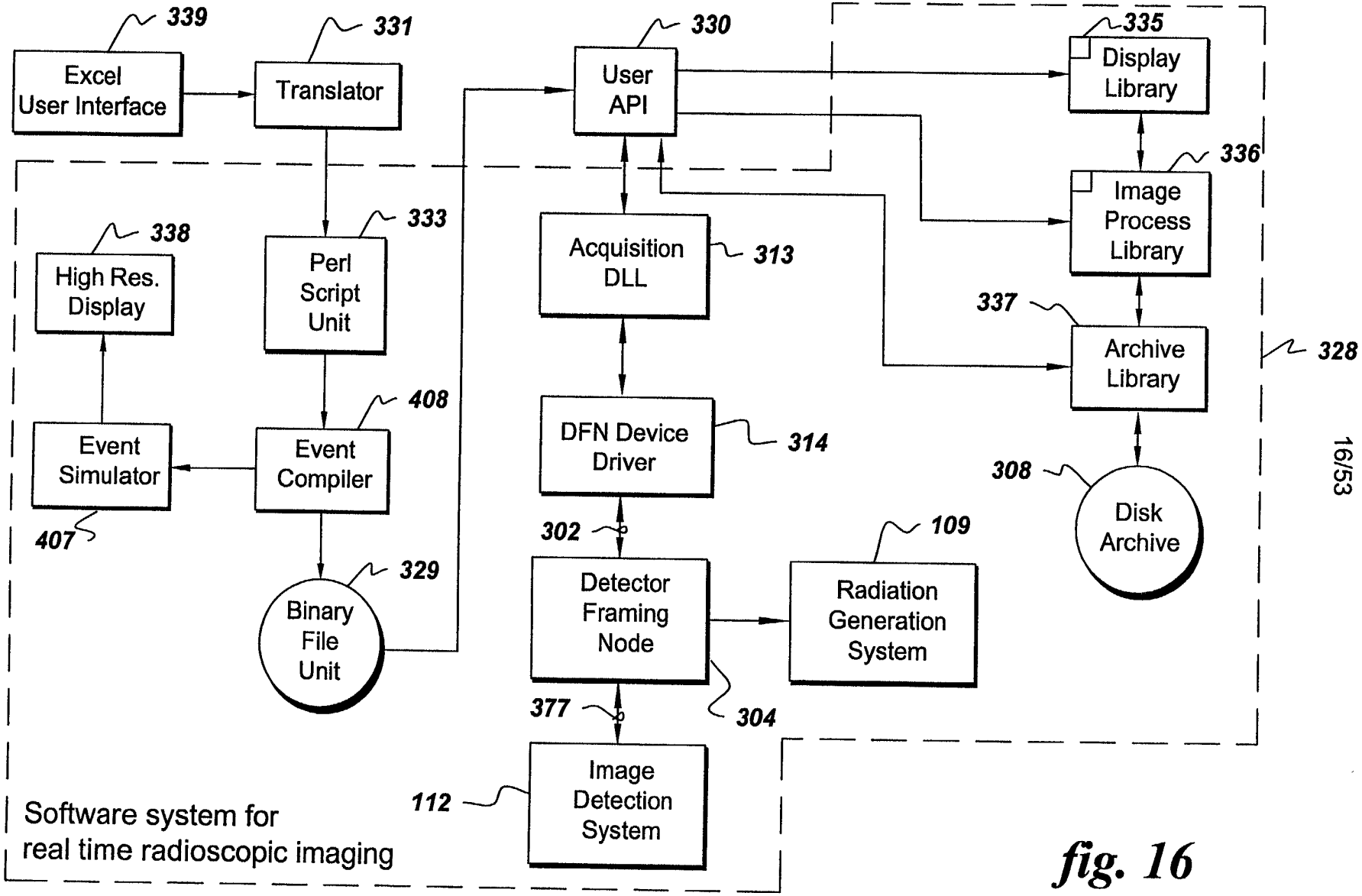
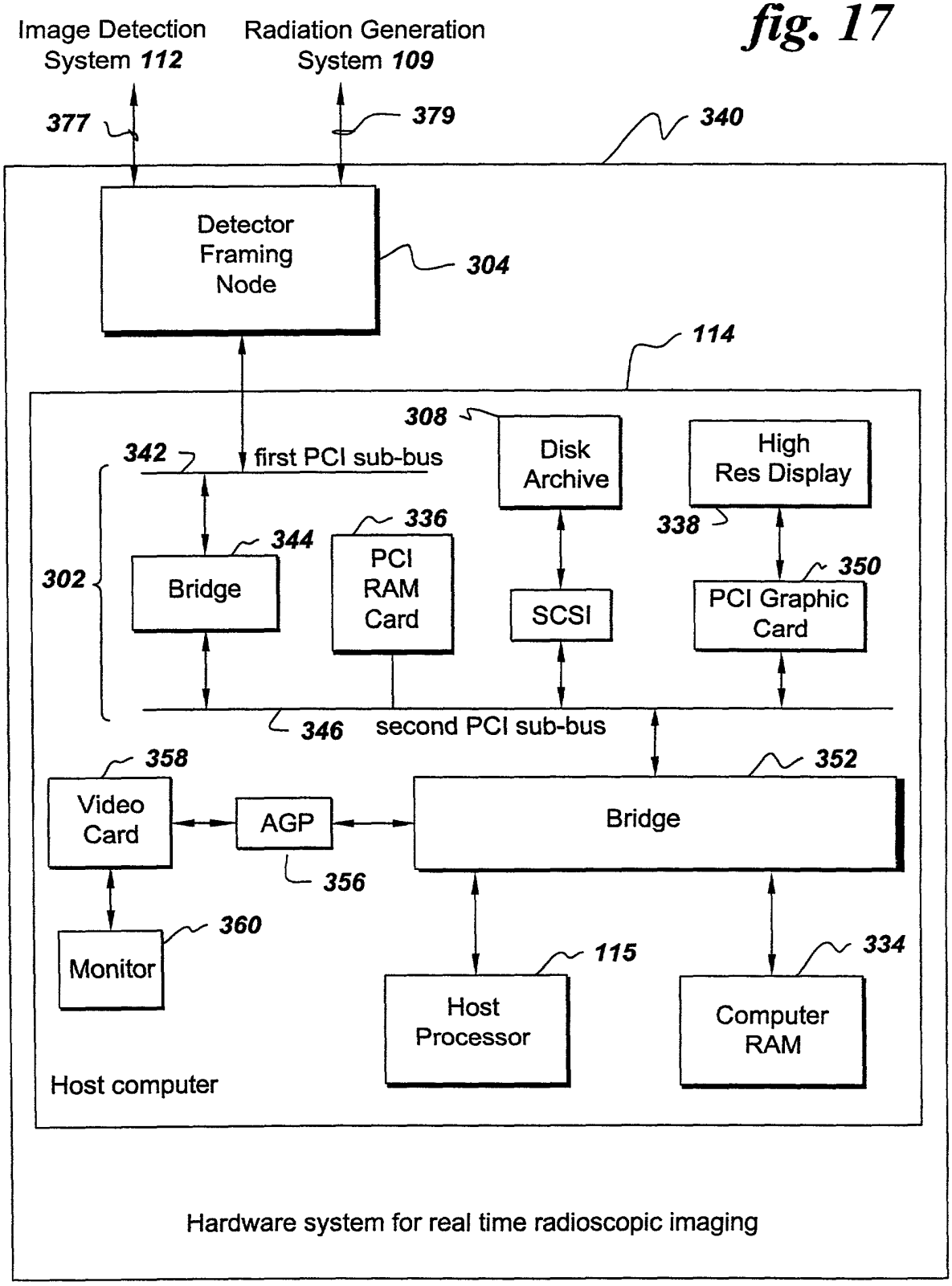

339
Excel User Interface
331
Translator
330
User API
335
Display Library
336
Image Process Library
333
Perl Script Unit
338
High Res. Display
Acquisition DLL
313
337
Archive Library
328
408
Event Compiler
Event Simulator
407
DFN Device Driver
314
308
Disk Archive
302
109
329
Binary File Unit
Detector Framing Node
Radiation Generation System
304
377
112
Image Detection System
Software system for real time radioscopic imaging

fig. 16

fig. 17



Hardware system for real time radioscopic imaging

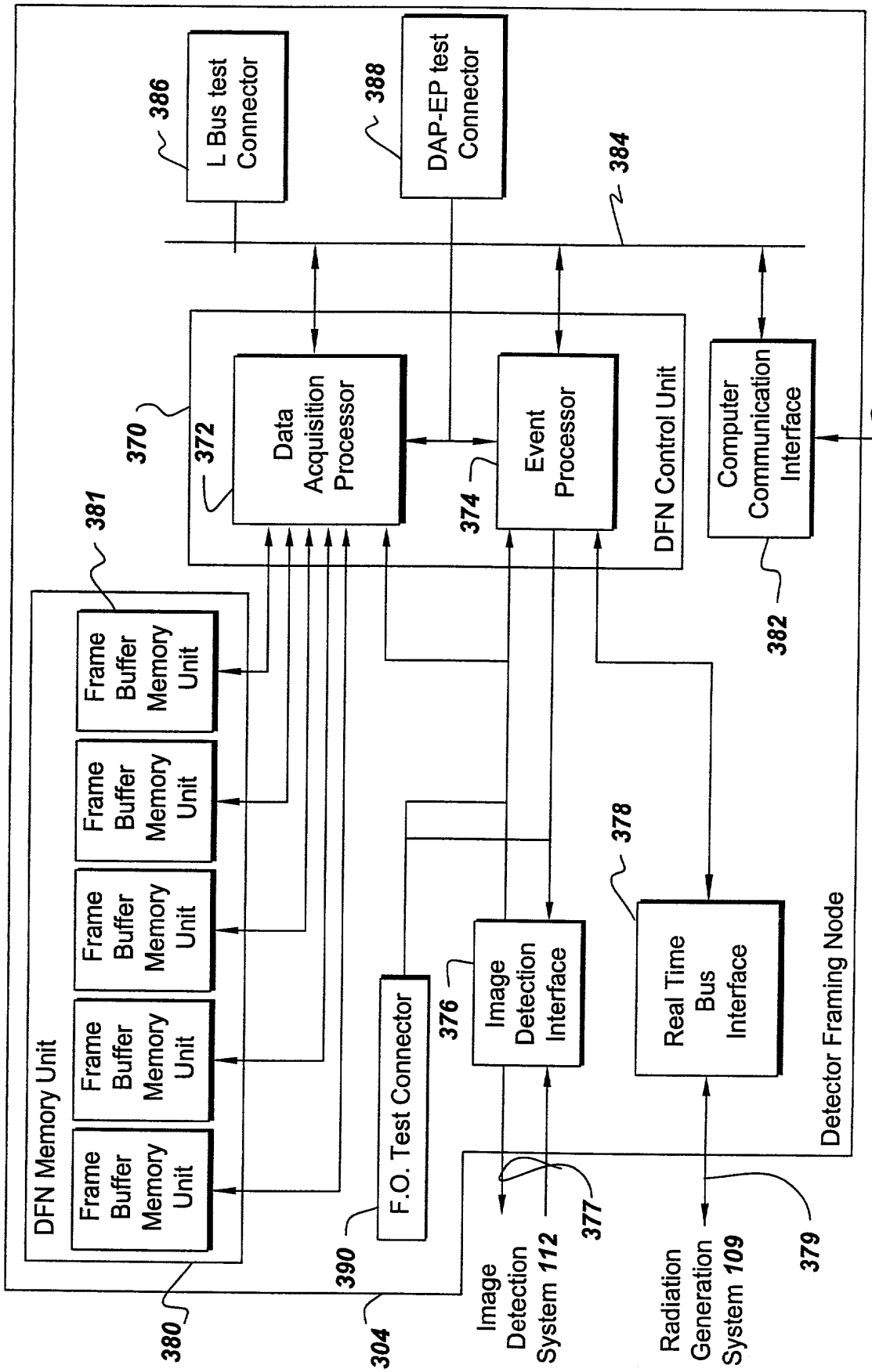

Detector Framing Node
DFN Memory Unit
Frame Buffer Memory Unit
Frame Buffer Memory Unit
Frame Buffer Memory Unit
Frame Buffer Memory Unit
Frame Buffer Memory Unit
381
380
304
390
F.O. Test Connector
376
Image Detection Interface
377
Image Detection System 112
378
Real Time Bus Interface
379
Radiation Generation System 109
370
DFN Control Unit
372
Data Acquisition Processor
374
Event Processor
382
Computer Communication Interface
302
Host Computer 114
384
386
L Bus test Connector
388
DAP-EP test Connector

fig. 18

		(fm/sec)	length	latency	memory	offset	gbr
Panel Setup	Real Time	30	unlimited	<5 frames	host	none	
Single Frame	Post Process	-	-	Delay ~.1 sec	"	y	
Single Frame	Post Process	-	-	Delay ~.2 sec	"	y	y
Real Time	Real Time	R	unlimited	<5 frames	host	none	
Real Time	Real Time	R-X	unlimited	<5 frames	"	y	
Real Time	Real Time	R-Y	unlimited	<5 frames	"	y	y

fig. 19

Modality	image size	Frames Stored host memory
Cardiac	1024 X 1024	200
Rad	2048 X 2048	50
Mammo	2304 X 2048	44

fig. 20

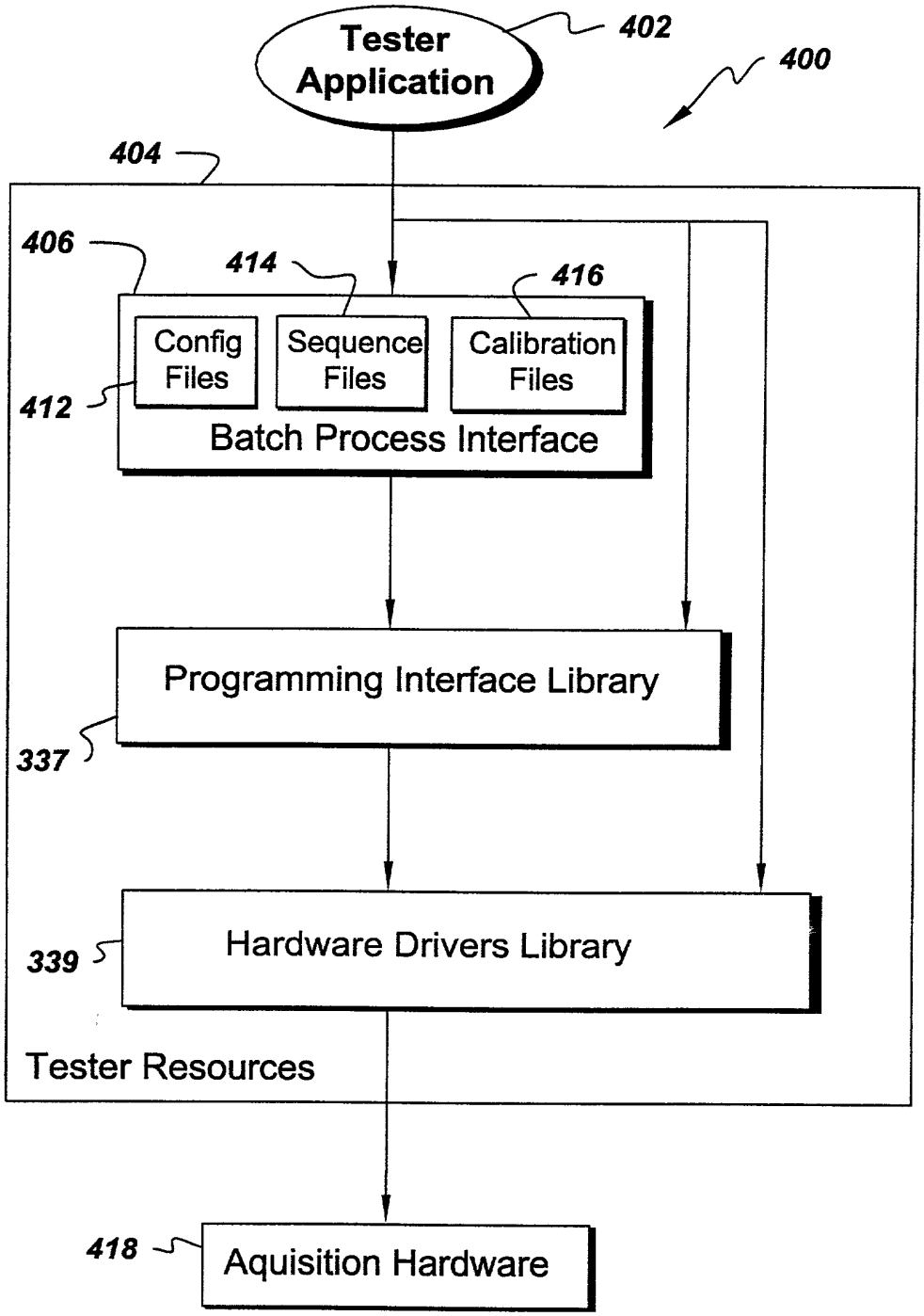

Tester Application
402
400
404
406
414
416
Config Files
Sequence Files
Calibration Files
412
Batch Process Interface
Programming Interface Library
337
339
Hardware Drivers Library
Tester Resources
418
Aquisition Hardware

fig. 21

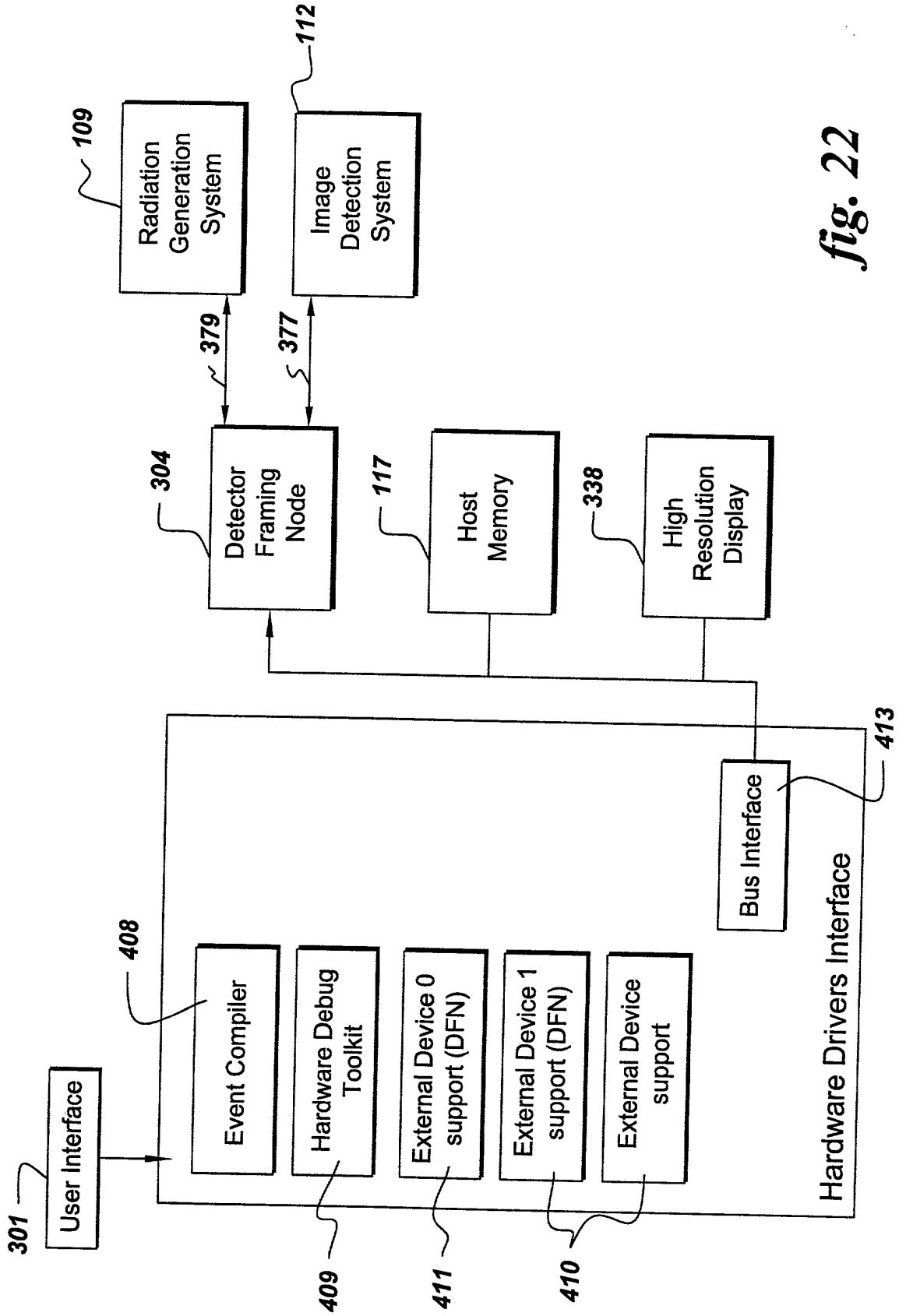

Radiation Generation System
109
Image Detection System
112
379
377
Detector Framing Node
304
Host Memory
117
High Resolution Display
338
Bus Interface
413
Hardware Drivers Interface
User Interface
301
Event Compiler
408
Hardware Debug Toolkit
409
External Device 0 support (DFN)
411
External Device 1 support (DFN)
External Device support
410

fig. 22

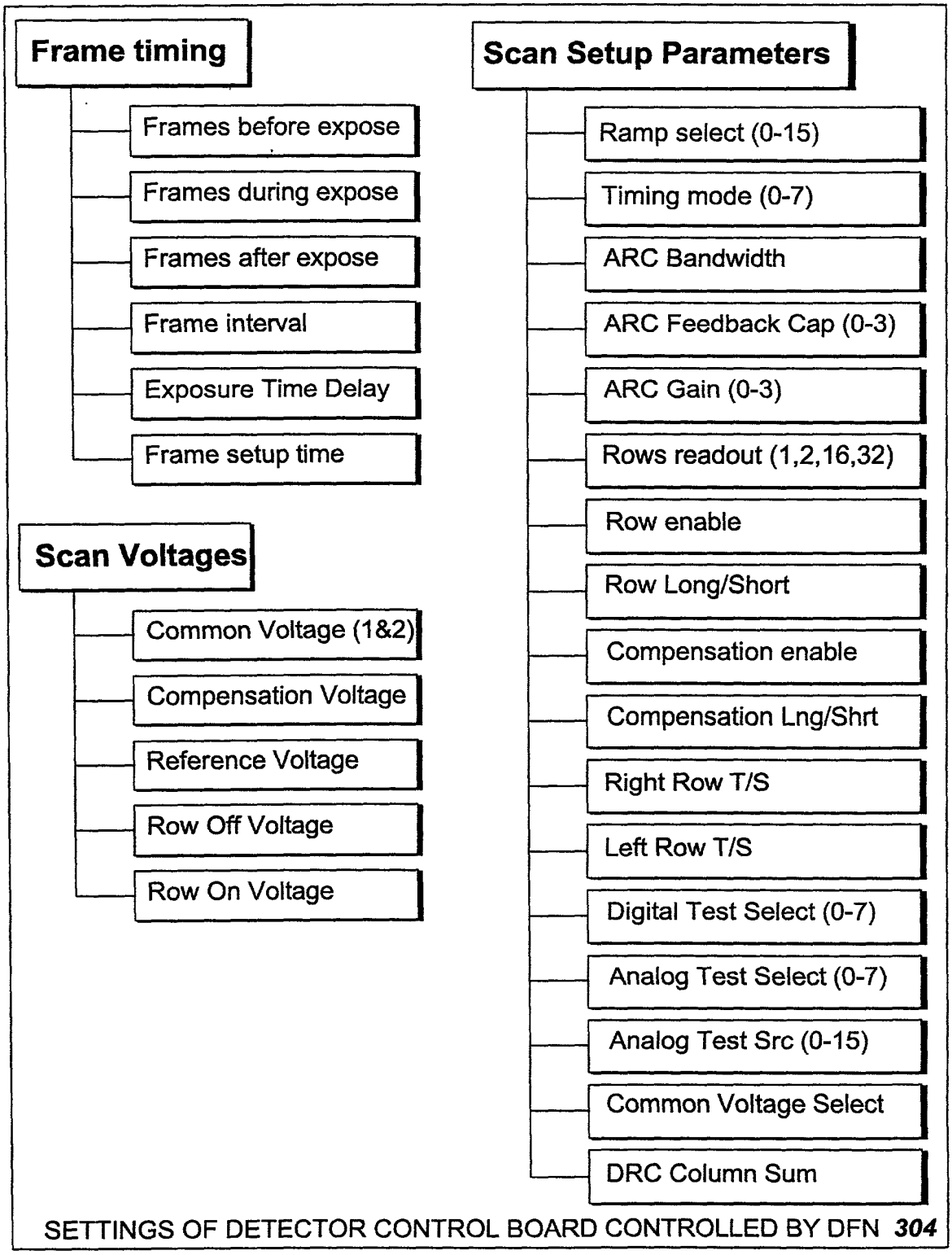

Frame timing
Frames before expose
Frames during expose
Frames after expose
Frame interval
Exposure Time Delay
Frame setup time
Scan Voltages
Common Voltage (1&2)
Compensation Voltage
Reference Voltage
Row Off Voltage
Row On Voltage
Scan Setup Parameters
Ramp select (0-15)
Timing mode (0-7)
ARC Bandwidth
ARC Feedback Cap (0-3)
ARC Gain (0-3)
Rows readout (1,2,16,32)
Row enable
Row Long/Short
Compensation enable
Compensation Lng/Shrt
Right Row T/S
Left Row T/S
Digital Test Select (0-7)
Analog Test Select (0-7)
Analog Test Src (0-15)
Common Voltage Select
DRC Column Sum
SETTINGS OF DETECTOR CONTROL BOARD CONTROLLED BY DFN 304

fig. 23

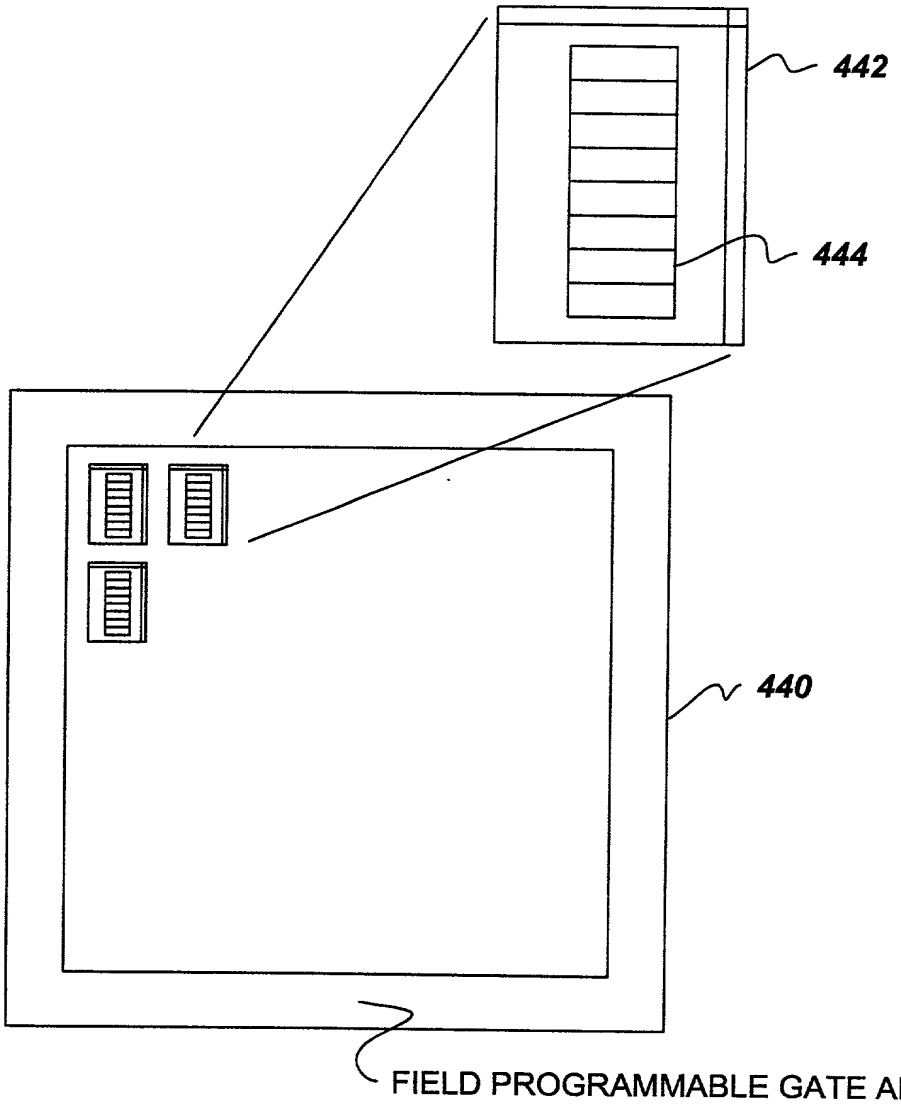


fig. 24

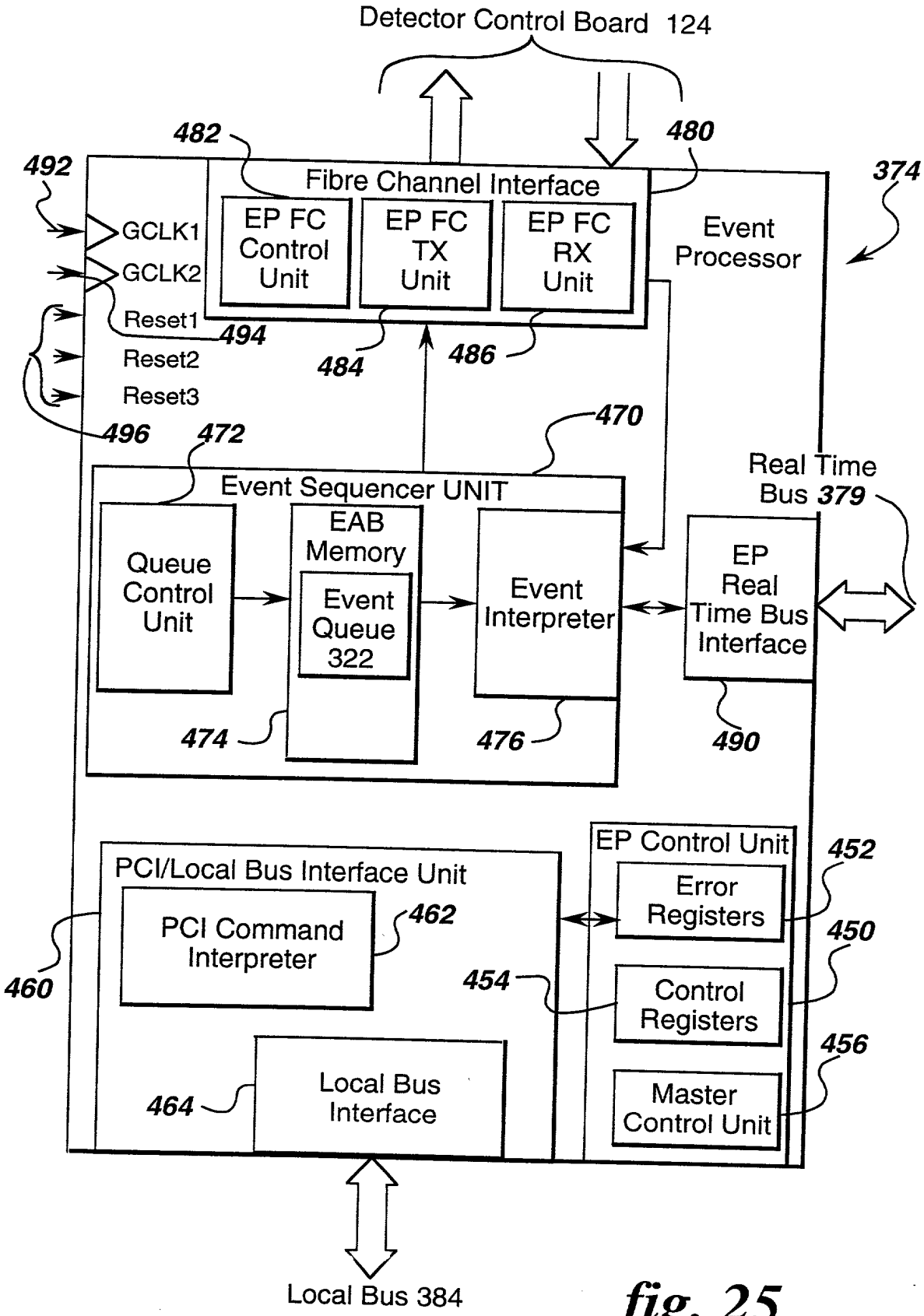

Detector Control Board 124
482
480
492
374
Fibre Channel Interface
EP FC Control Unit
EP FC TX Unit
EP FC RX Unit
Event Processor
GCLK1
GCLK2
Reset1
Reset2
Reset3
494
484
486
496
472
470
Event Sequencer UNIT
Queue Control Unit
EAB Memory
Event Queue 322
Event Interpreter
Real Time Bus 379
EP Real Time Bus Interface
474
476
490
EP Control Unit
452
PCI/Local Bus Interface Unit
PCI Command Interpreter
462
460
454
Error Registers
Control Registers
450
456
Local Bus Interface
464
Master Control Unit
Local Bus 384

fig. 25

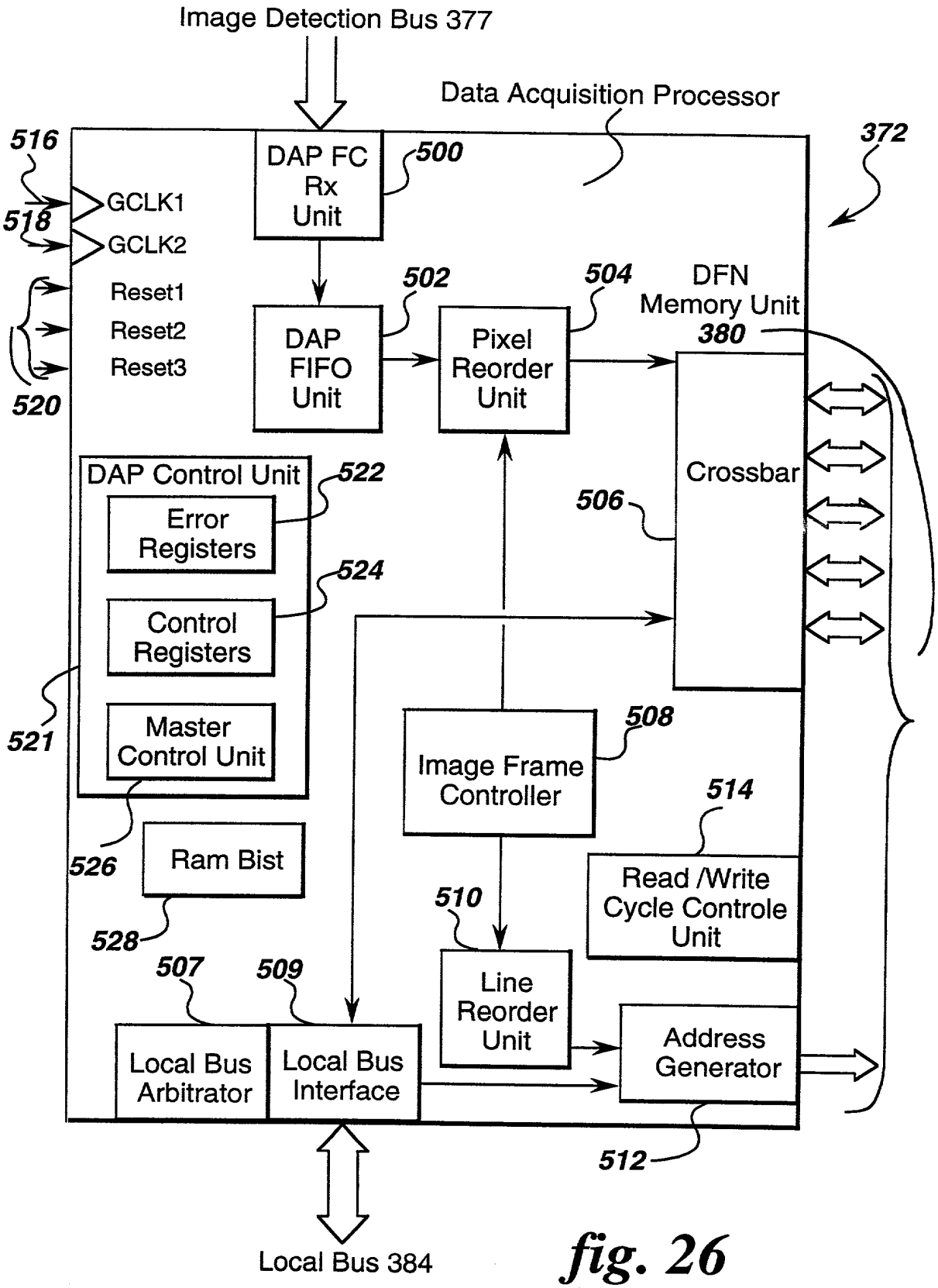


Image Detection Bus 377
Data Acquisition Processor
372
516
518
GCLK1
GCLK2
Reset1
Reset2
Reset3
520
DAP FC Rx Unit
500
DAP FIFO Unit
502
Pixel Reorder Unit
504
DFN Memory Unit
380
Crossbar
506
DAP Control Unit
522
Error Registers
524
Control Registers
521
Master Control Unit
526
Ram Bist
528
Image Frame Controller
508
514
Read /Write Cycle Controle Unit
510
Line Reorder Unit
507
509
Local Bus Arbitrator
Local Bus Interface
Address Generator
512
Local Bus 384

fig. 26

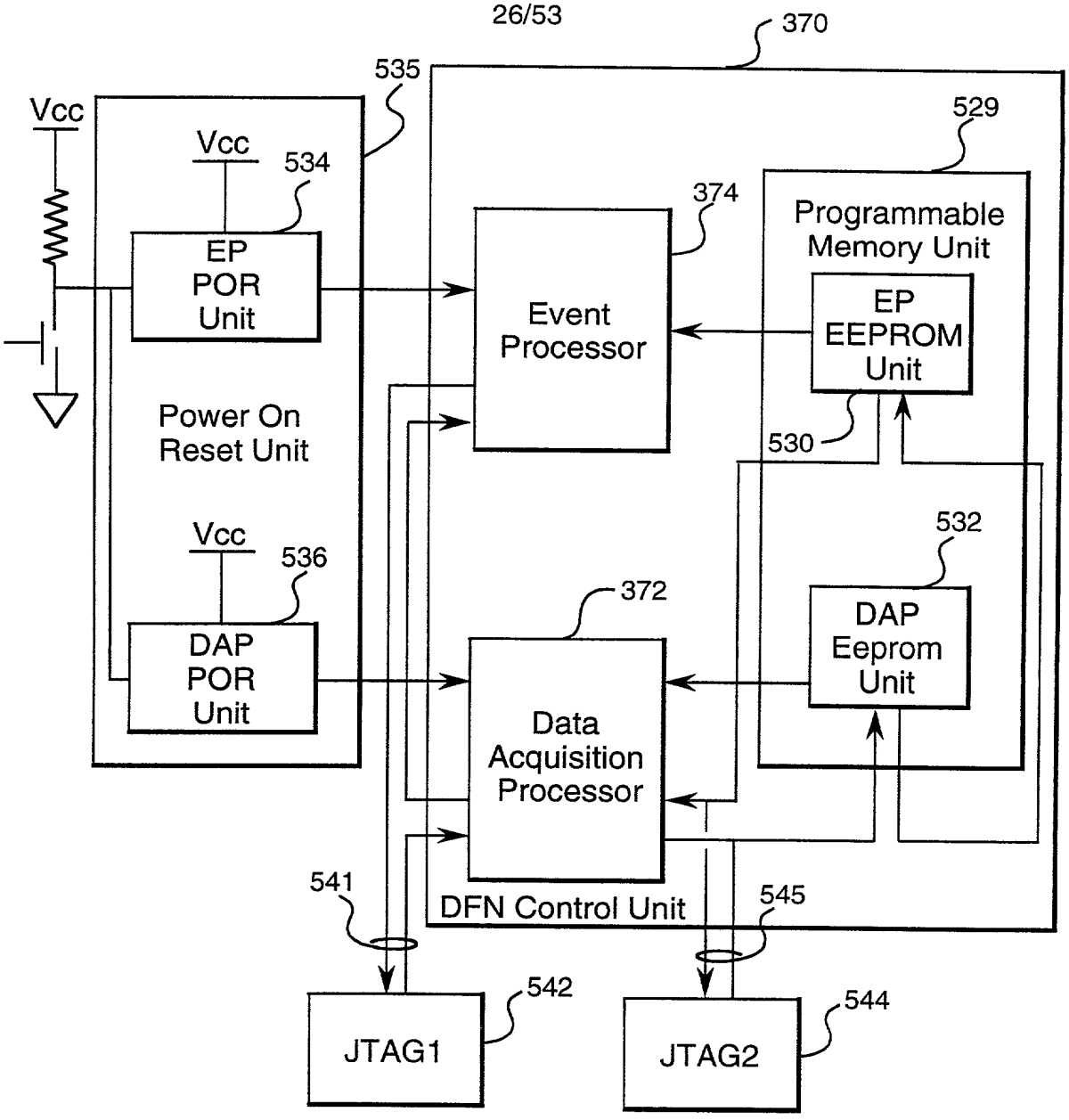

370
535
Vcc
Vcc
534
529
374
EP
POR
Unit
Event
Processor
Programmable
Memory Unit
EP
EEPROM
Unit
530
Power On
Reset Unit
Vcc
536
532
372
DAP
POR
Unit
DAP
Eeprom
Unit
Data
Acquisition
Processor
541
DFN Control Unit
545
542
544
JTAG1
JTAG2

fig. 27

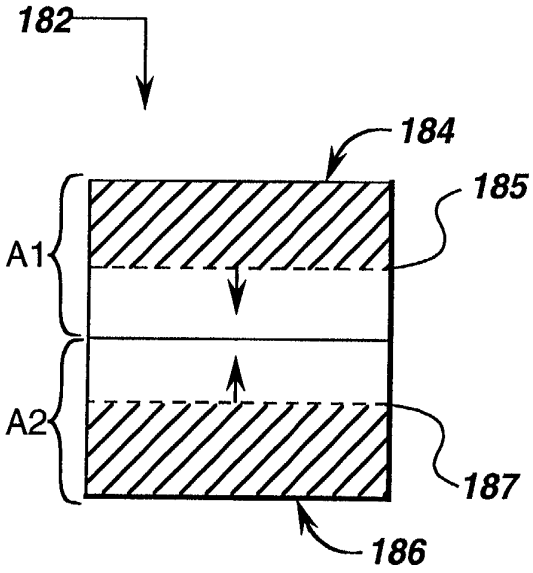


fig. 28

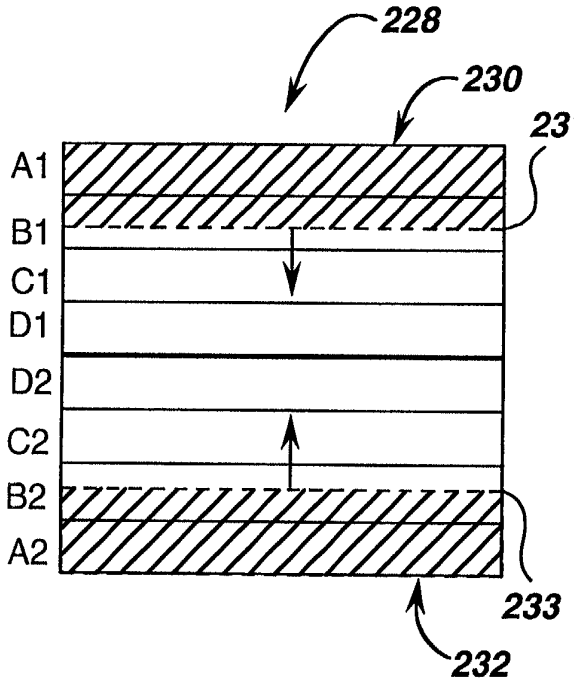


fig. 29

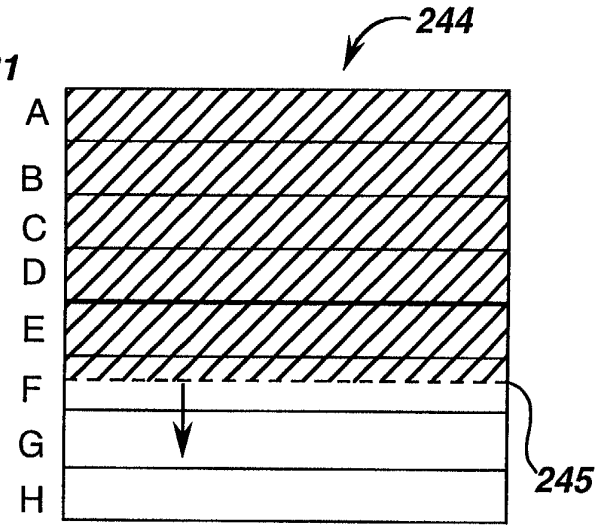


fig. 30

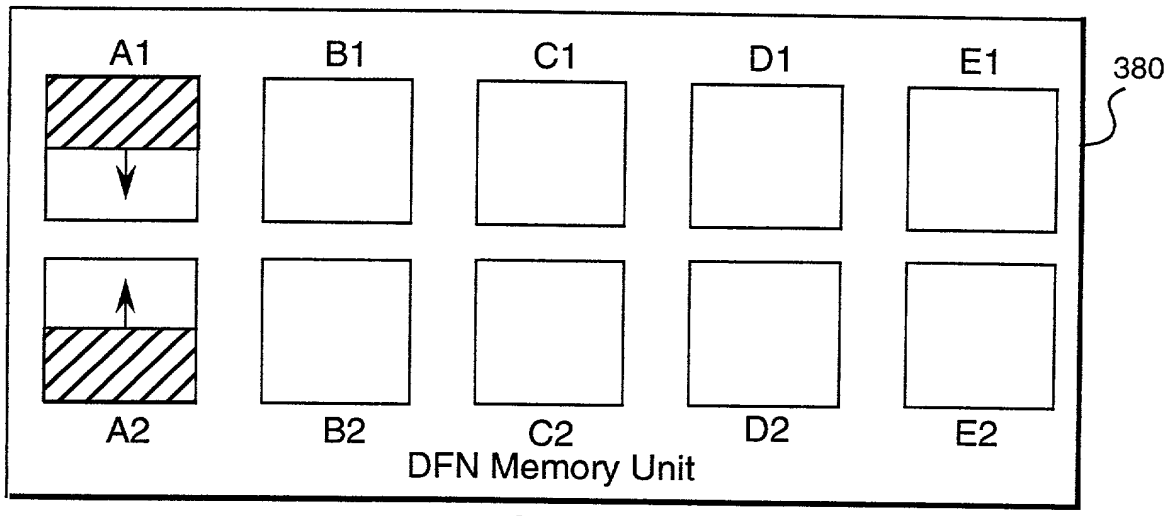


fig. 31

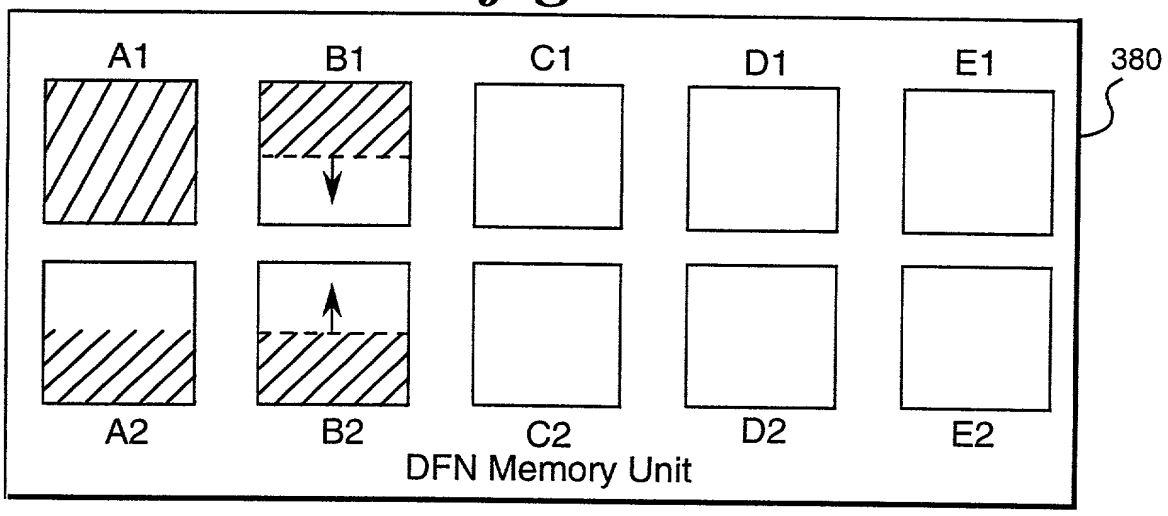


fig. 32

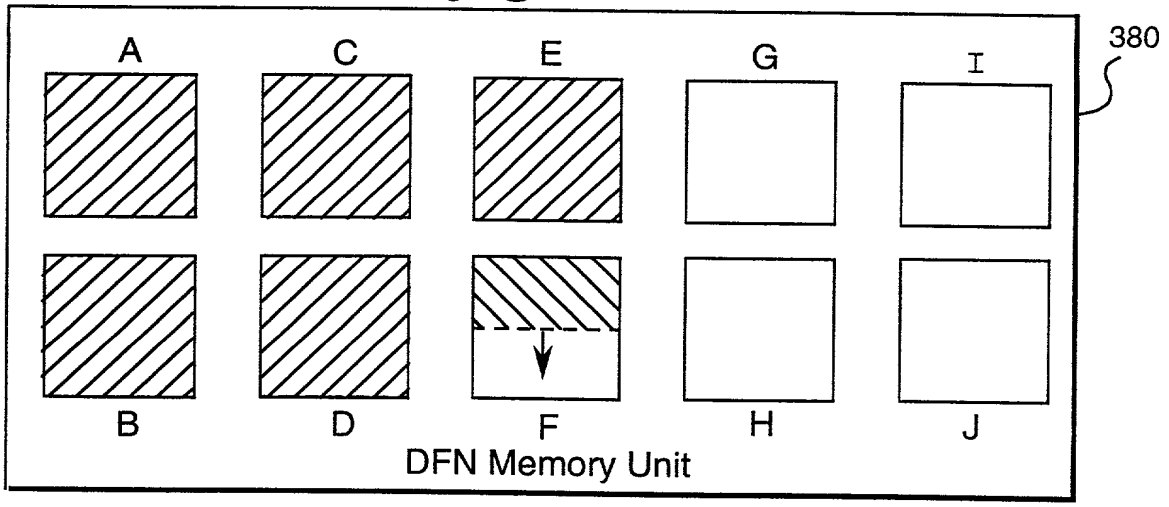


fig. 33

FOUND SATISFIED

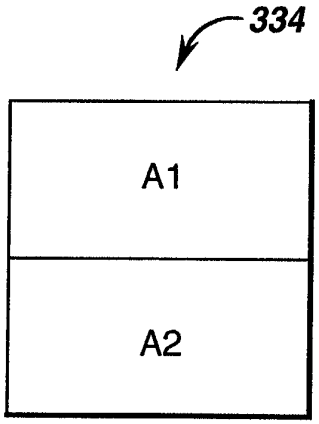


fig. 34

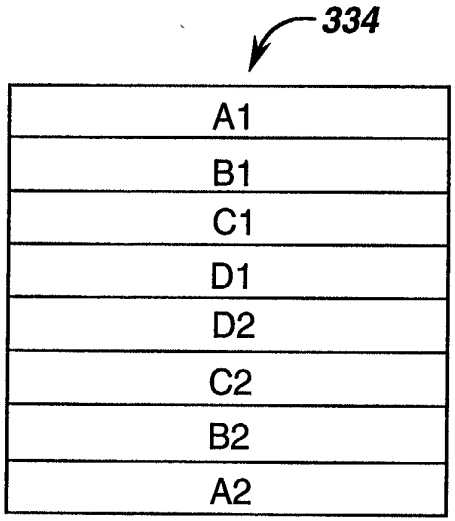


fig. 35

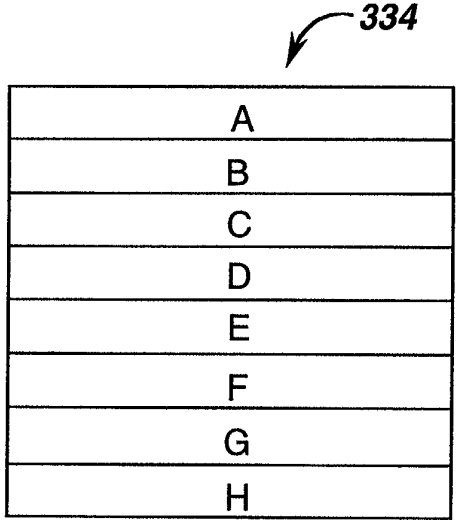


fig. 36

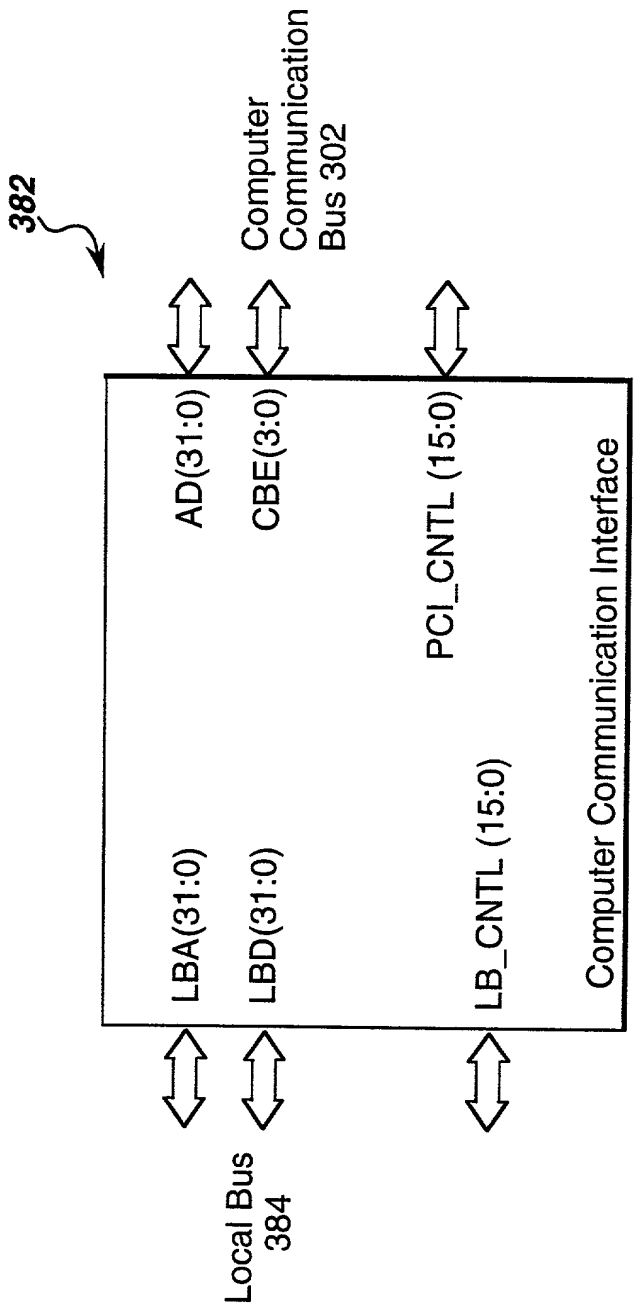

382
Computer Communication Bus 302
AD(31:0)
CBE(3:0)
PCI_CNTL (15:0)
LBA(31:0)
LBD(31:0)
LB_CNTL (15:0)
Computer Communication Interface
Local Bus 384

fig. 37

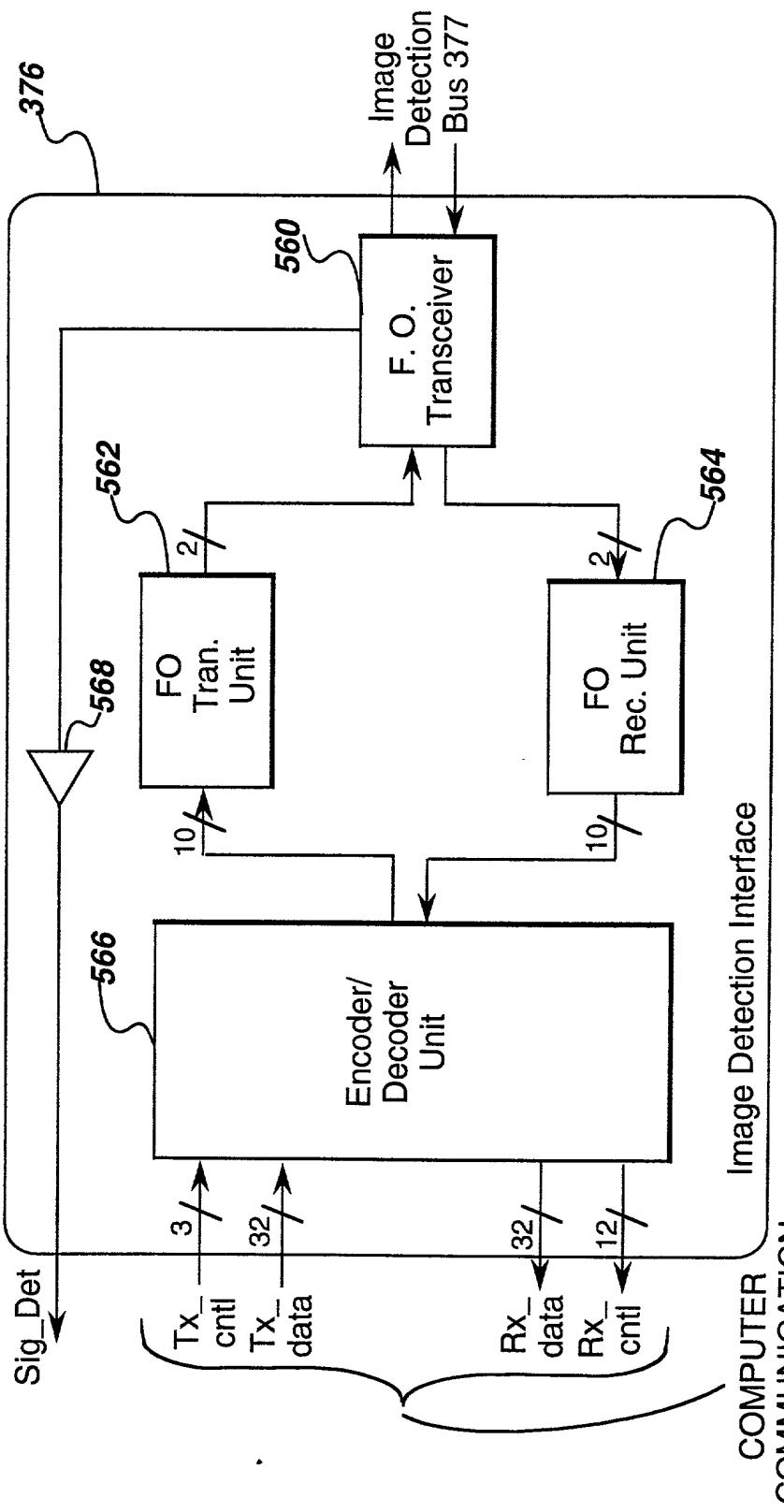

376
Image Detection Bus 377
560
F. O. Transceiver
562
564
2
2
FO Tran. Unit
FO Rec. Unit
568
10
10
566
Encoder/ Decoder Unit
3
32
32
12
Image Detection Interface
Sig_Det
Tx_ cntl
Tx_ data
Rx_ data
Rx_ cntl
COMPUTER COMMUNICATION Bus 302

fig. 38

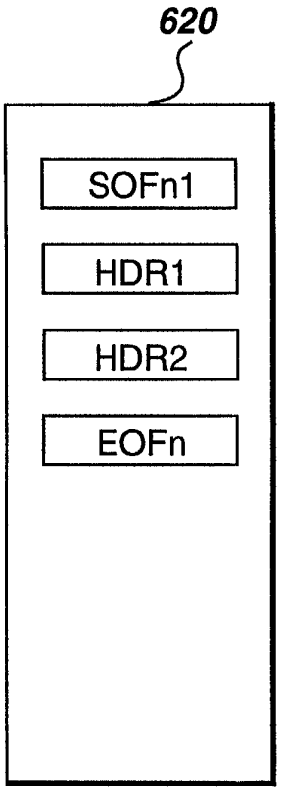


fig. 39

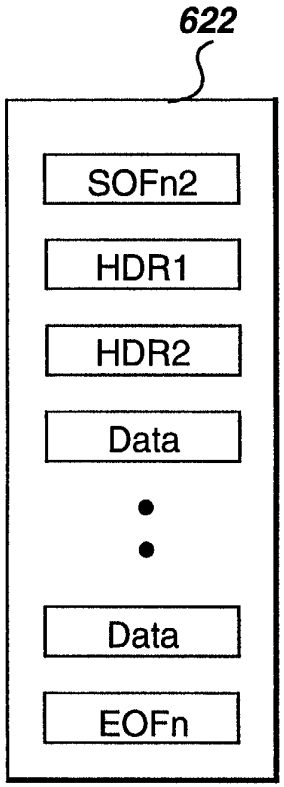


fig. 40

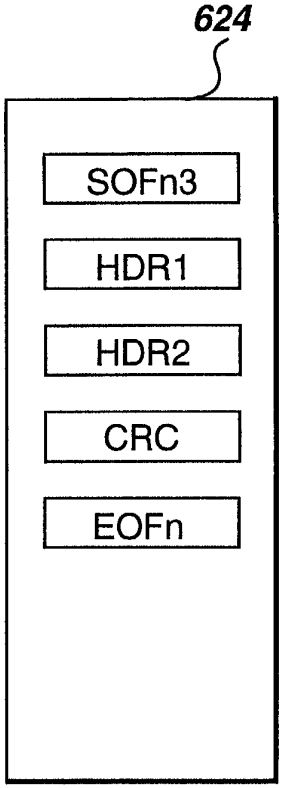


fig. 41

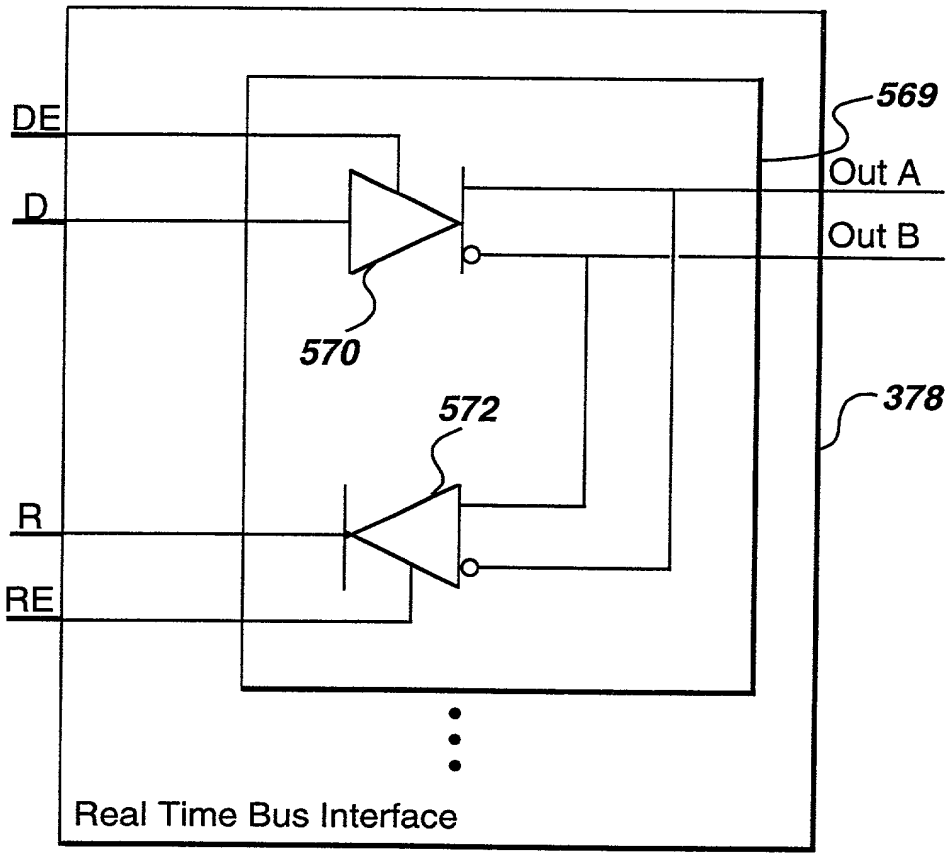


fig. 42

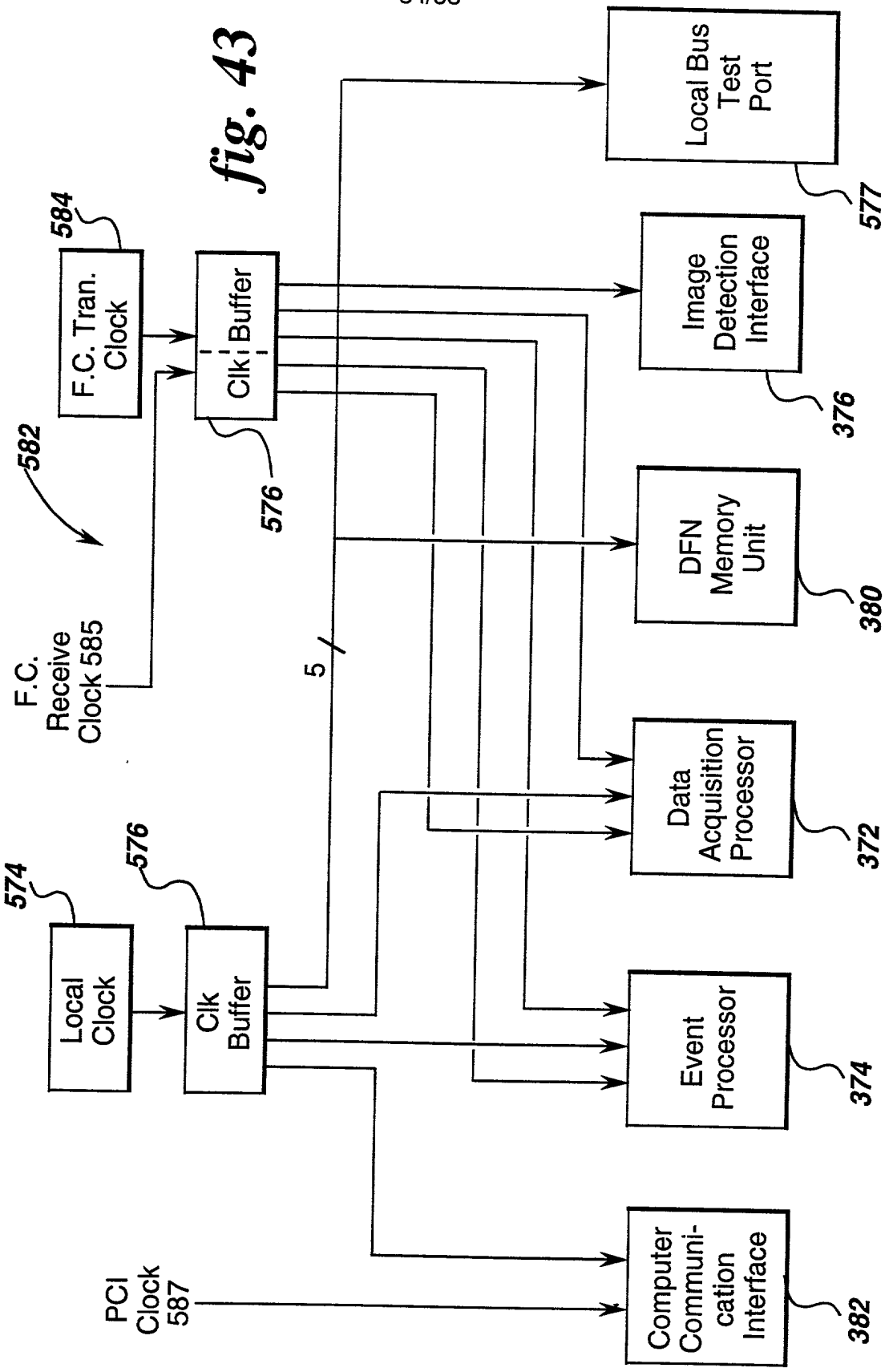

Local Bus Test Port
577
Image Detection Interface
376
DFN Memory Unit
380
Data Acquisition Processor
372
Event Processor
374
Computer Communi-cation Interface
382
Local Clock
574
Clk Buffer
576
F.C. Tran. Clock
584
Clk Buffer
576
582
F.C. Receive Clock 585
PCI Clock 587
5

fig. 43

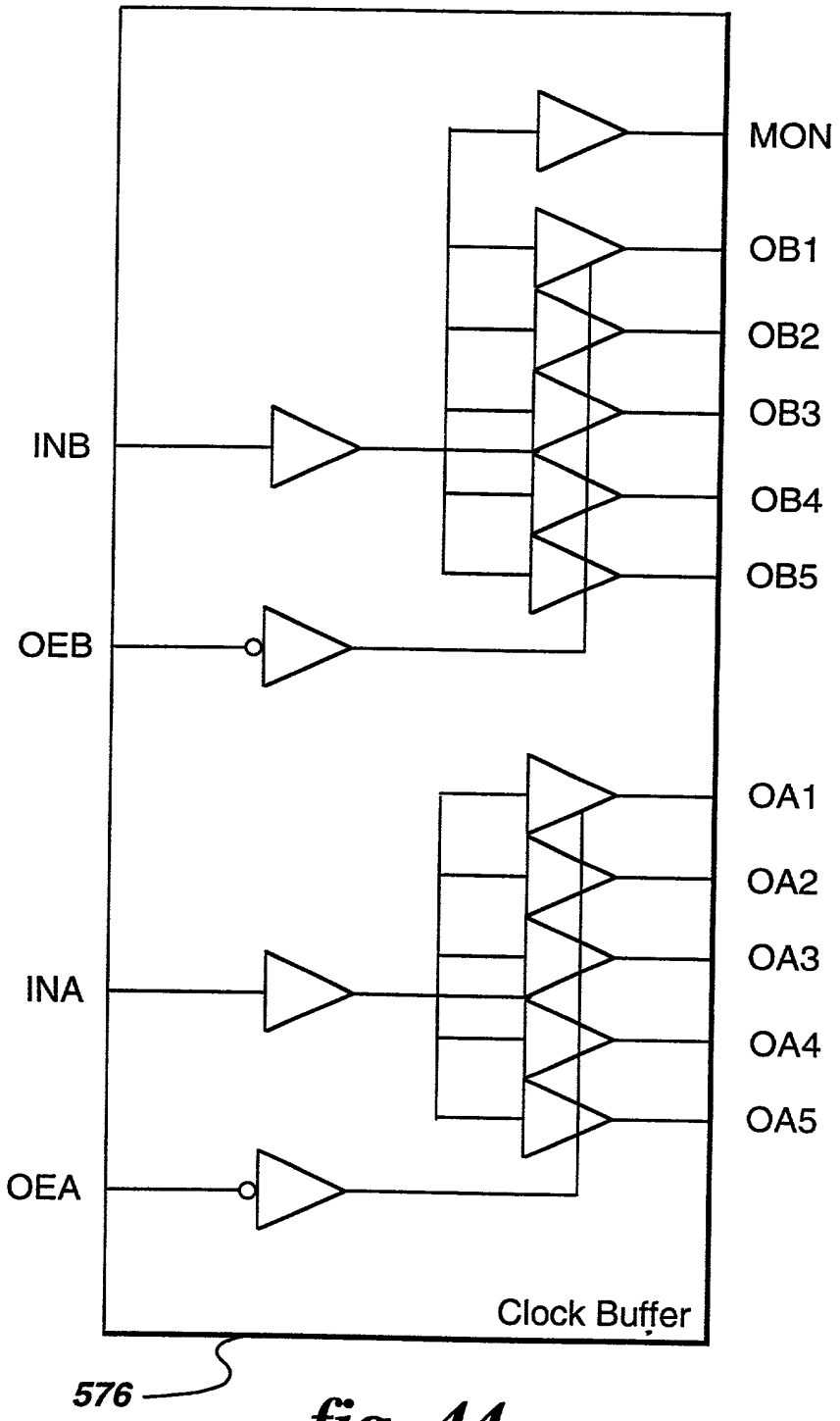

MON
OB1
OB2
OB3
OB4
OB5
INB
OEB
OA1
OA2
OA3
OA4
OA5
INA
OEA
Clock Buffer
576

fig. 44

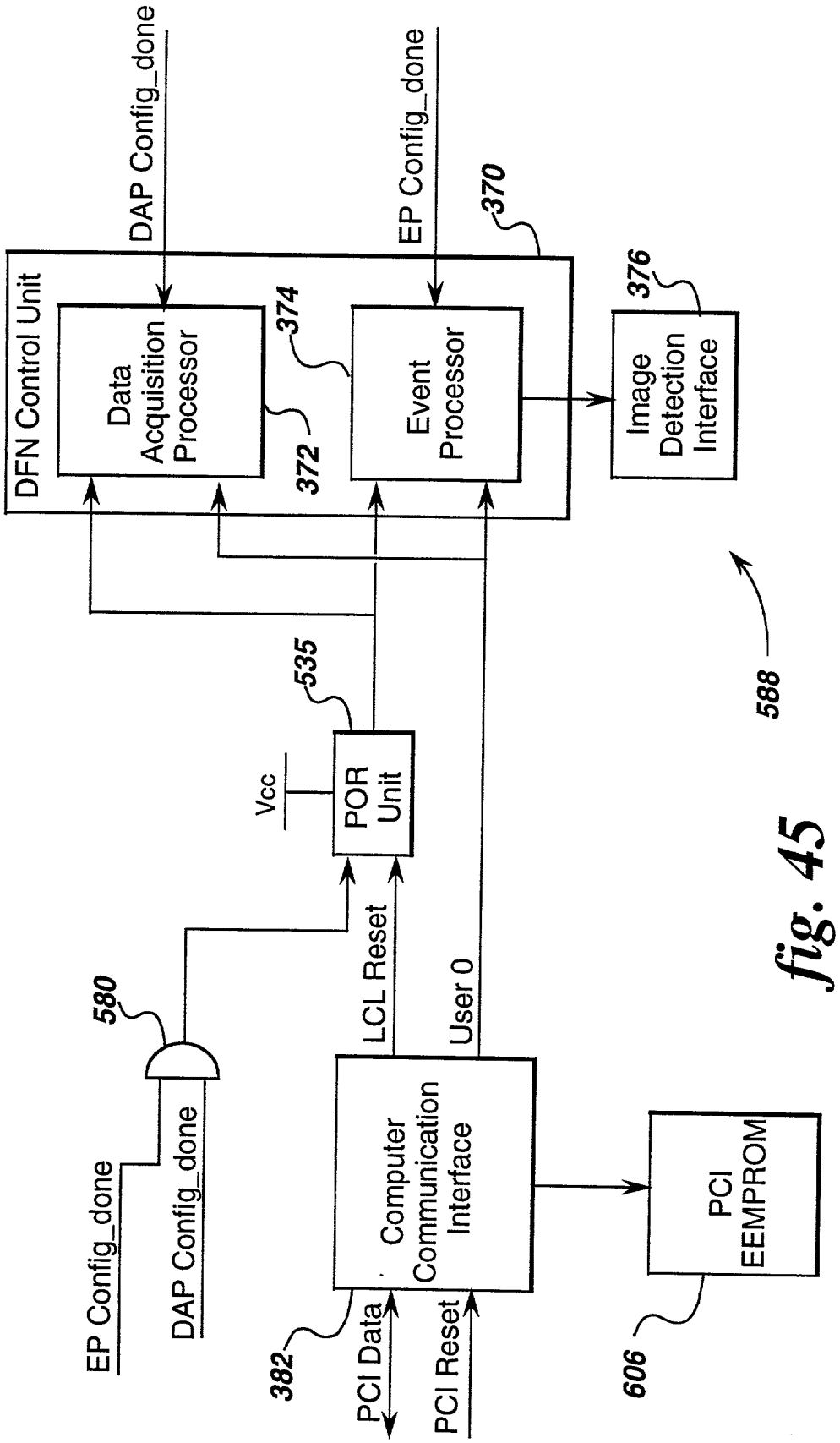

DFN Control Unit
DAP Config_done
EP Config_done
370
Data Acquisition Processor
374
372
Event Processor
376
Image Detection Interface
588
535
Vcc
POR Unit
580
LCL Reset
User 0
EP Config_done
DAP Config_done
Computer Communication Interface
382
PCI Data
PCI Reset
606
PCI EEPROM

fig. 45

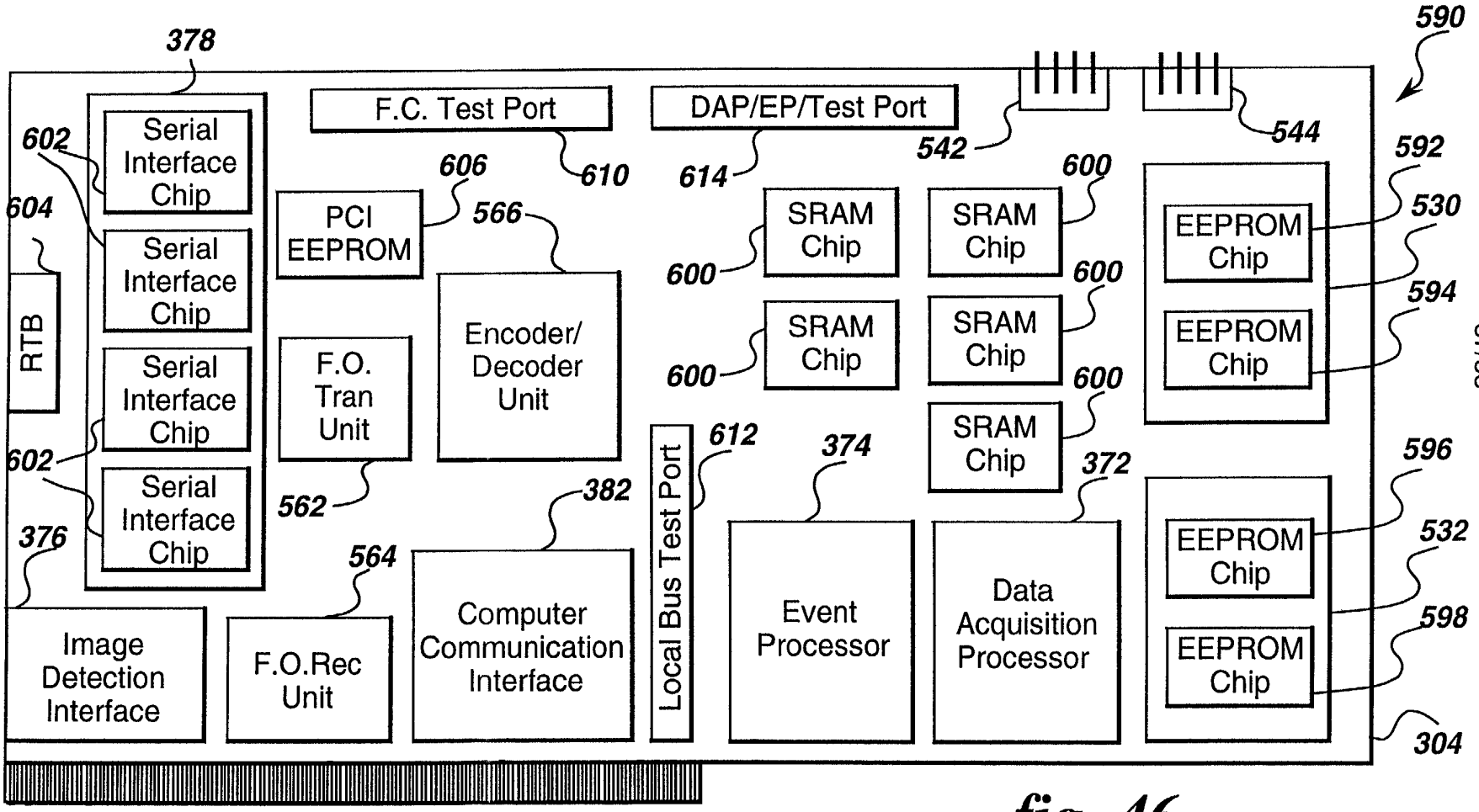
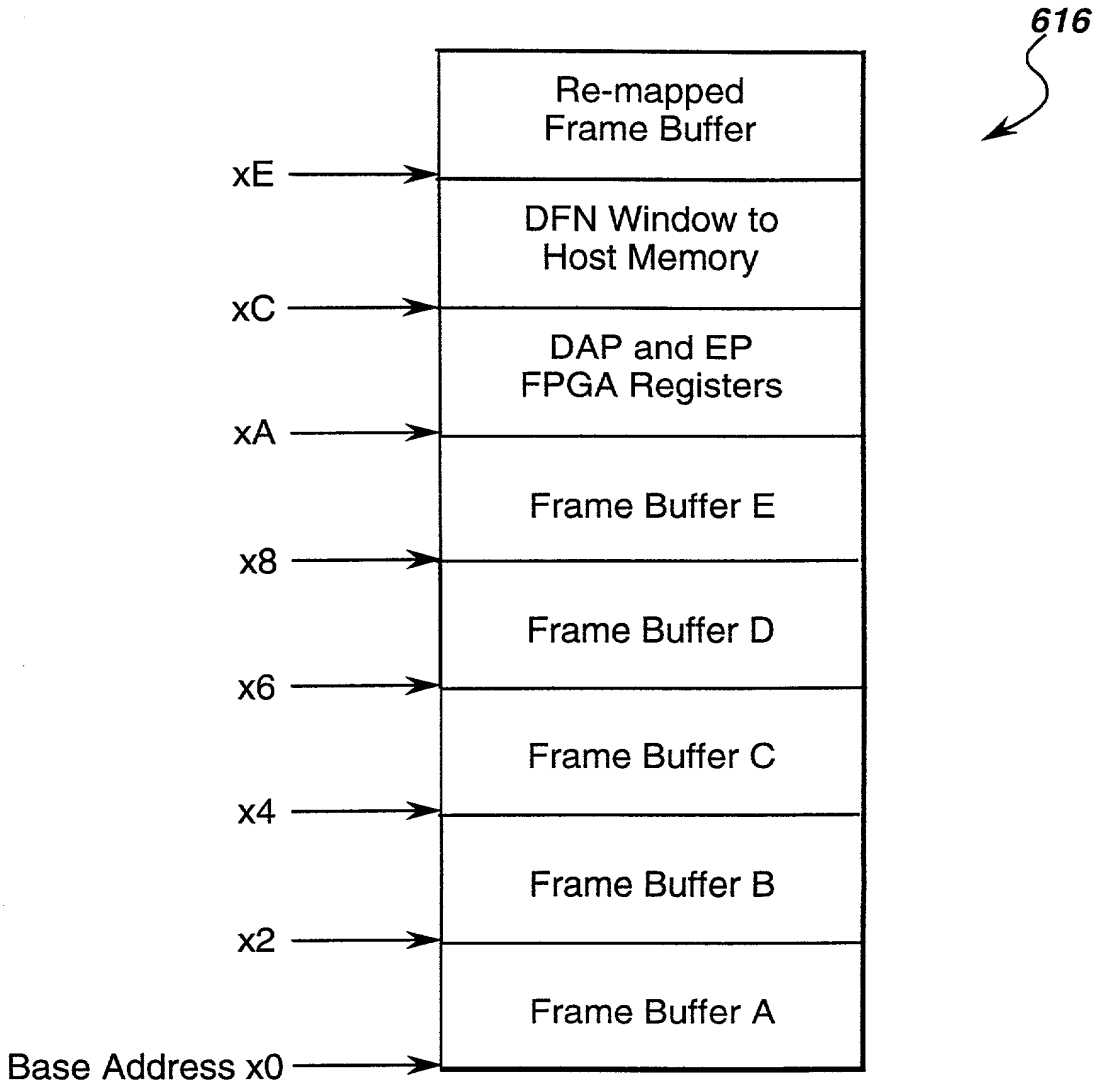

378
590
602
Serial Interface Chip
Serial Interface Chip
Serial Interface Chip
Serial Interface Chip
604
RTB
F.C. Test Port
610
DAP/EP/Test Port
614
542
544
606
PCI EEPROM
566
Encoder/ Decoder Unit
F.O. Tran Unit
562
600
SRAM Chip
SRAM Chip
SRAM Chip
SRAM Chip
SRAM Chip
SRAM Chip
592
EEPROM Chip
EEPROM Chip
530
594
612
Local Bus Test Port
374
372
382
376
564
Image Detection Interface
F.O.Rec Unit
Computer Communication Interface
Event Processor
Data Acquisition Processor
596
EEPROM Chip
EEPROM Chip
532
598
304

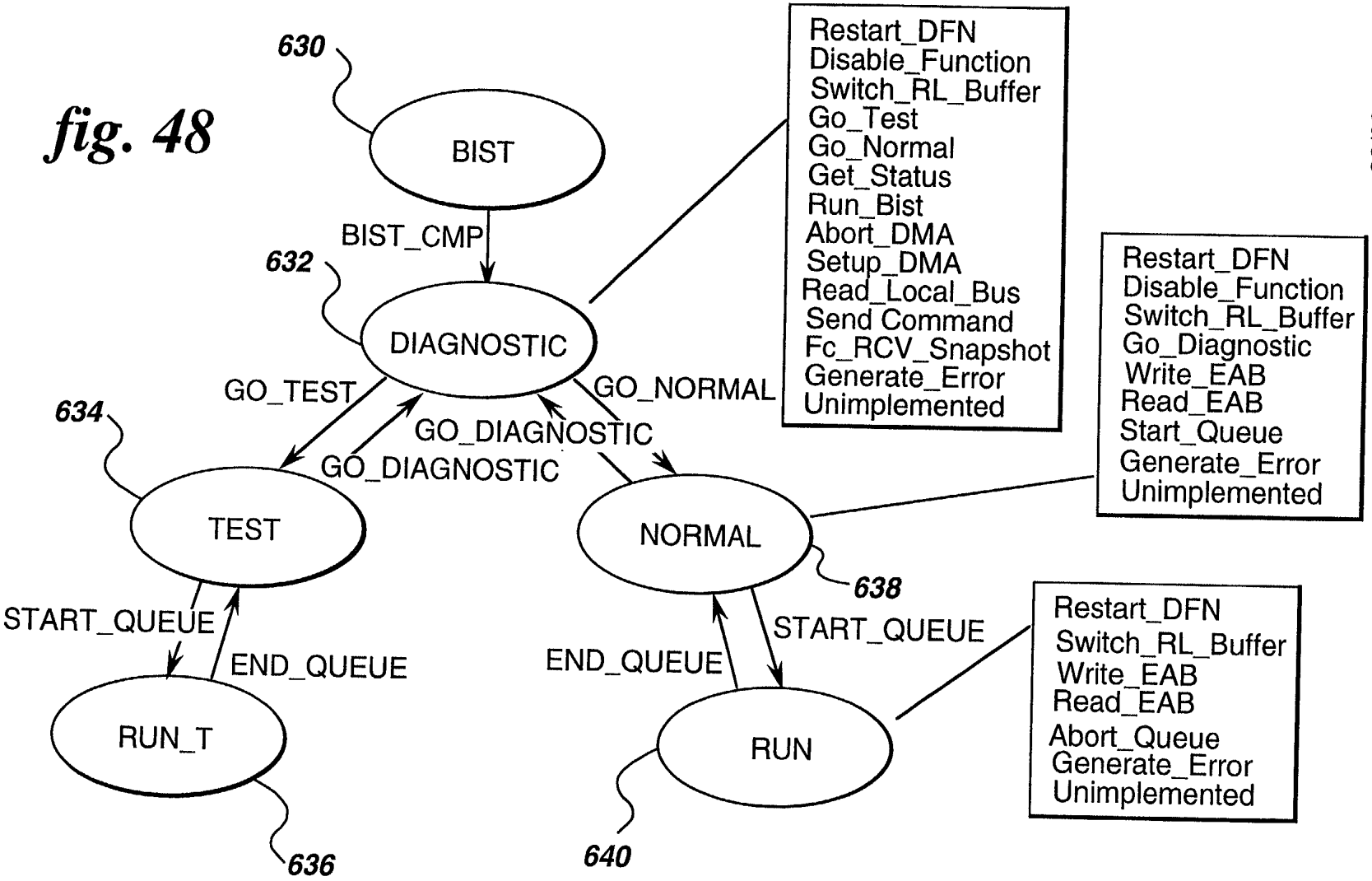
fig. 46



Mapping of 16 MByte PCI Address Space

fig. 47

fig. 48


630
BIST
BIST_CMP
632
DIAGNOSTIC
GO_TEST
GO_DIAGNOSTIC
GO_DIAGNOSTIC
GO_NORMAL
634
TEST
START_QUEUE
END_QUEUE
RUN_T
636
NORMAL
638
START_QUEUE
END_QUEUE
RUN
640
Restart_DFN
Disable_Function
Switch_RL_Buffer
Go_Test
Go_Normal
Get_Status
Run_Bist
Abort_DMA
Setup_DMA
Read_Local_Bus
Send Command
Fc_RCV_Snapshot
Generate_Error
Unimplemented
Restart_DFN
Disable_Function
Switch_RL_Buffer
Go_Diagnostic
Write_EAB
Read_EAB
Start_Queue
Generate_Error
Unimplemented
Restart_DFN
Switch_RL_Buffer
Write_EAB
Read_EAB
Abort_Queue
Generate_Error
Unimplemented

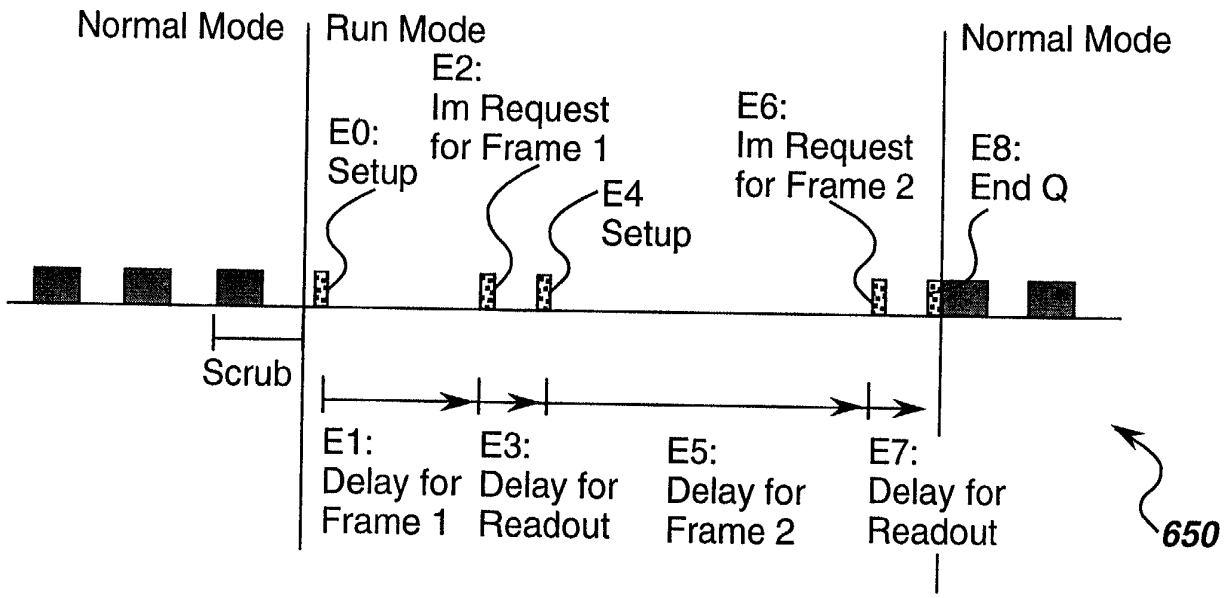

Normal Mode
Run Mode
Normal Mode
E2:
Im Request
for Frame 1
E0:
Setup
E6:
Im Request
for Frame 2
E8:
End Q
E4
Setup
Scrub
E1:
Delay for
Frame 1
E3:
Delay for
Readout
E5:
Delay for
Frame 2
E7:
Delay for
Readout
650

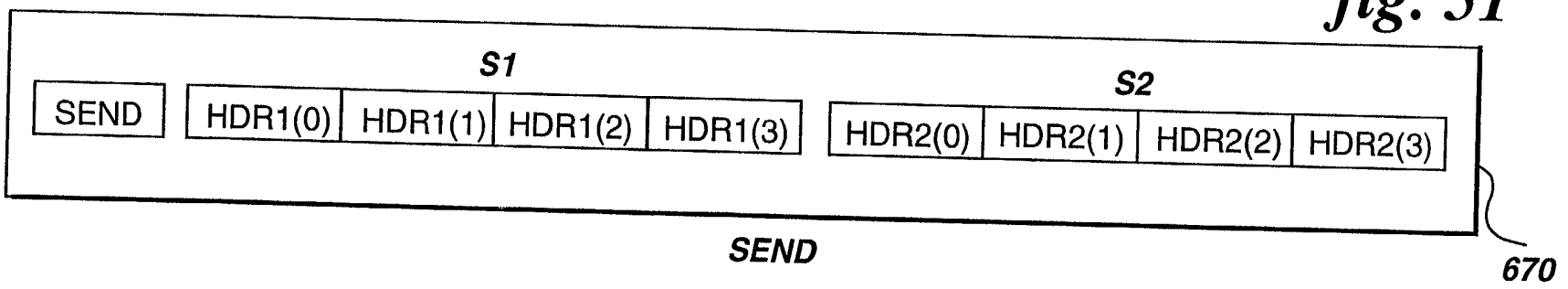
fig. 49

Event Mnemonic	Event (showing size of arguments)	Op Code (hex)	Data (bytes)	Total (bytes)
Endq	Endq	14	0	1
Delay (T)	Delay (0xff ff ff ff)	10	4	5
Send (command, value)	Send (0xff ff ff ff, 0xff ff ff ff)	04	8	9
LoopKN (K, N)	LoopKN (0xff ff, 0xff)	0C	3	4
LoopKF (K, F)	LoopKF (0xff ff, 0xff ff ff)	0D	5	6
Wait (F)	Wait (0xff ff, ff)	09	3	4
Flag (F)	Flag (0xff ff, ff)	08	3	4

660

fig. 50

fig. 51



Error Mnemonic	Description of Error
FC_TIMEOUT	Timeout Expired With No ACK Detected
FC_BAD_ACK	ACK Did Not Match Transmitted Command
FC_EXTRA_ACK	Unexpected ACK Received
FC_EXTRA_CMD	New Send Event While Waiting for ACK From Previous Send
SIG_DETN	No Input Signal Power on Fibre Channel (Cable Disconnected?)
RXERROR	Fibre Channel Receiver Detected Bad Data (Defective Chipset?)
WRDSYNCN	Fibre Channel Data Link Unsynchronized
CRXS(1)	Bad Received CRC Detected (Fiber-optic Cable Problem?)
CRXS(3) & CRXS(2)	Bad Order in Link State Machine (Defective Chipset?)

672

fig. 52

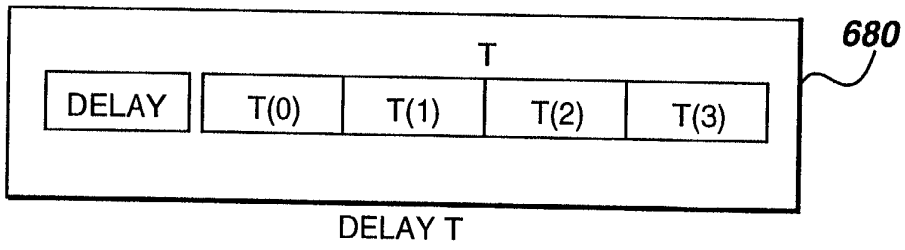


fig. 53

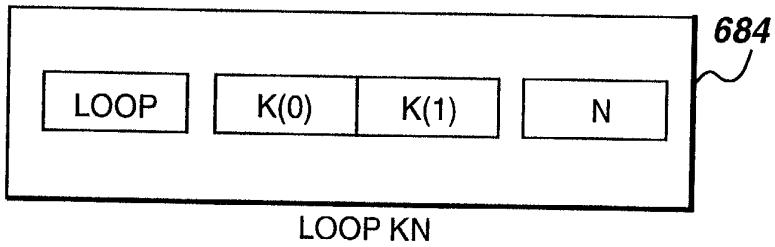


fig. 54

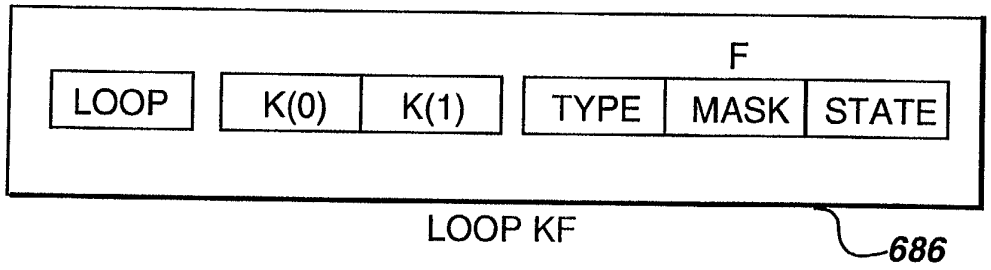


fig. 55

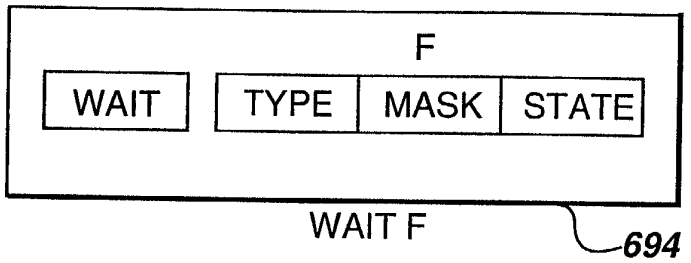


fig. 56

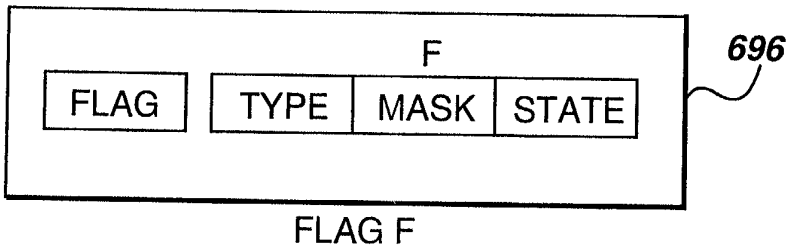


fig. 57

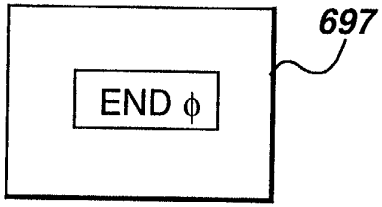


fig. 58

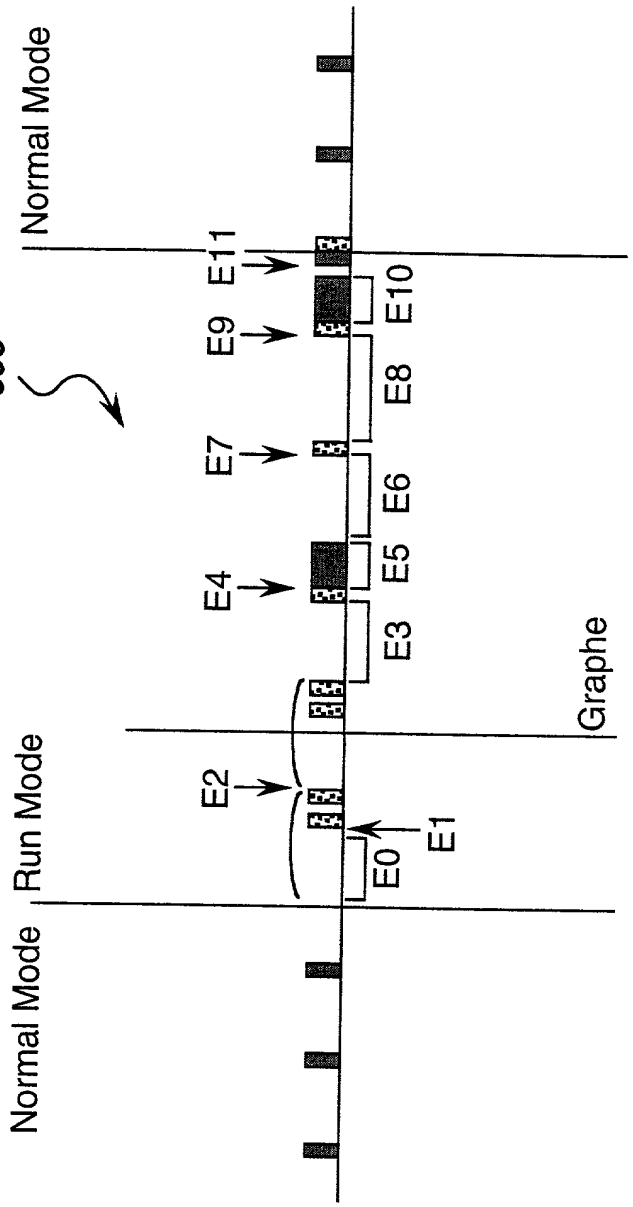

Normal Mode
698
E11
E9
E10
E8
E7
E6
E5
E4
E3
Graphe
E2
E1
E0
Run Mode
Normal Mode

fig. 59

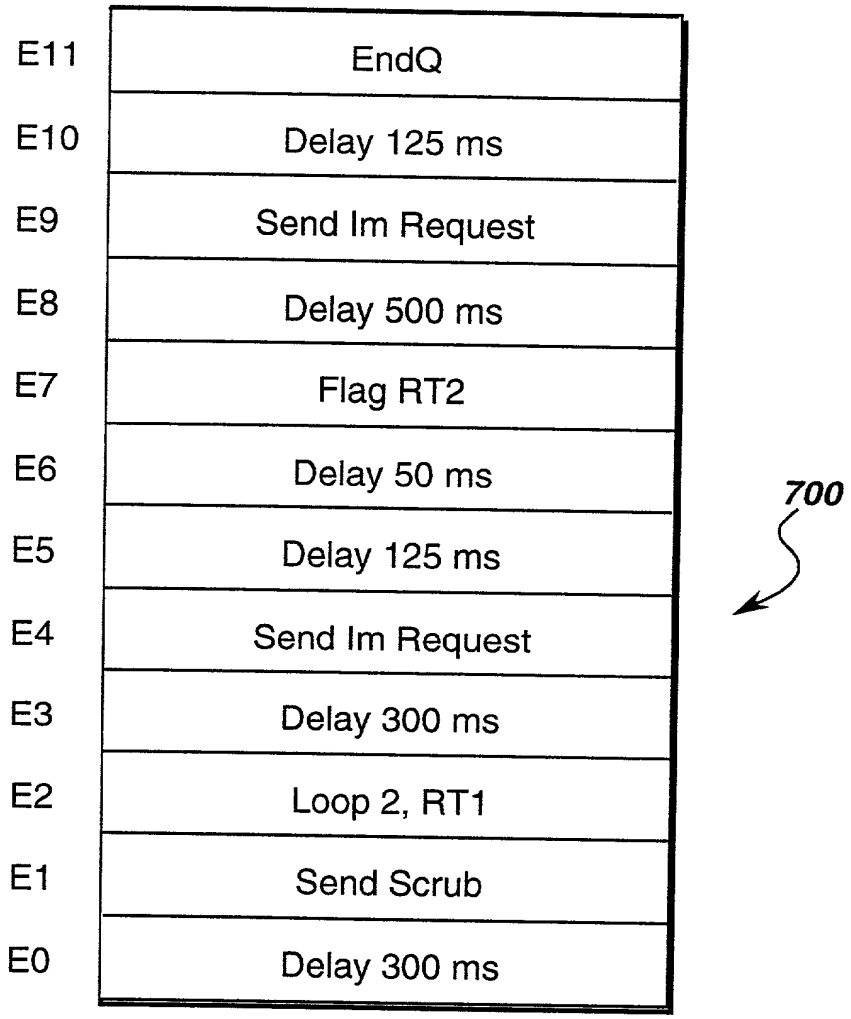

E11
EndQ
E10
Delay 125 ms
E9
Send Im Request
E8
Delay 500 ms
E7
Flag RT2
E6
Delay 50 ms
E5
Delay 125 ms
E4
Send Im Request
E3
Delay 300 ms
E2
Loop 2, RT1
E1
Send Scrub
E0
Delay 300 ms
700
EVENT QUEUE

fig. 60

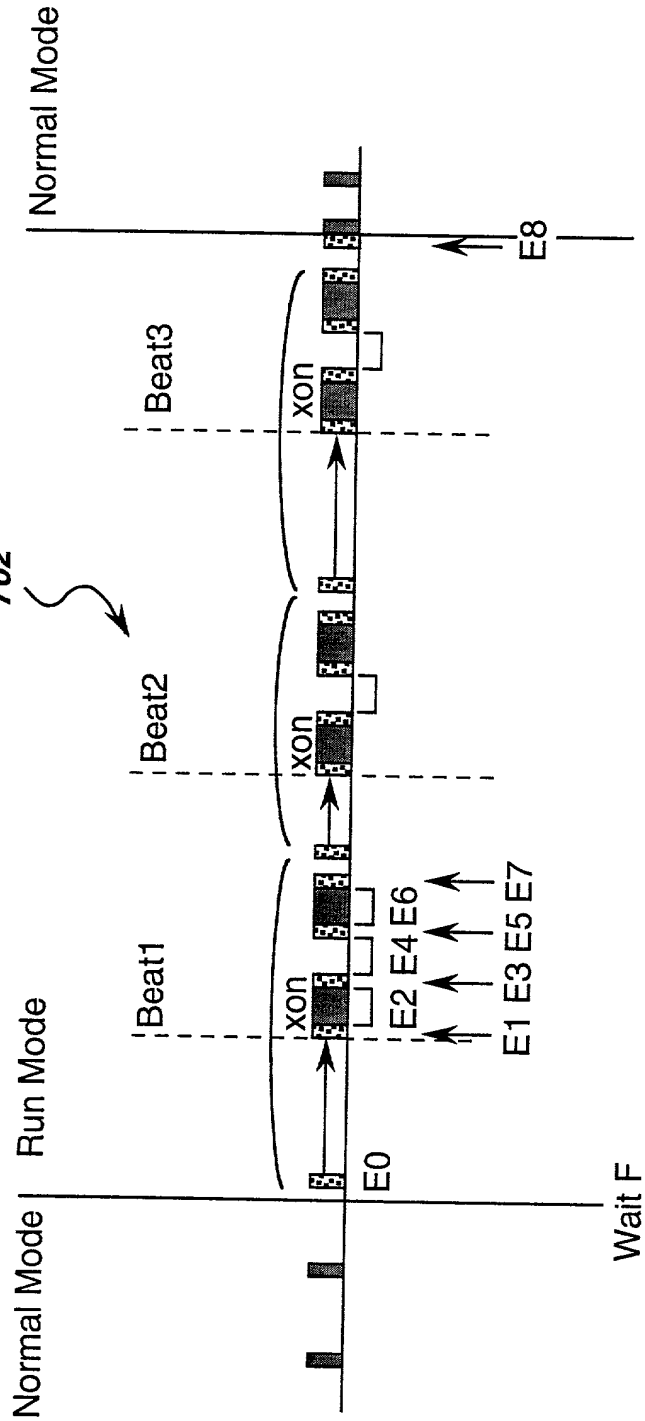

Normal Mode
Run Mode
Normal Mode
Wait F
Wait For Beat
E0
E1 E3 E5 E7
E2 E4 E6
E8
Beat1
Beat2
Beat3
xon
xon
xon
702

fig. 61

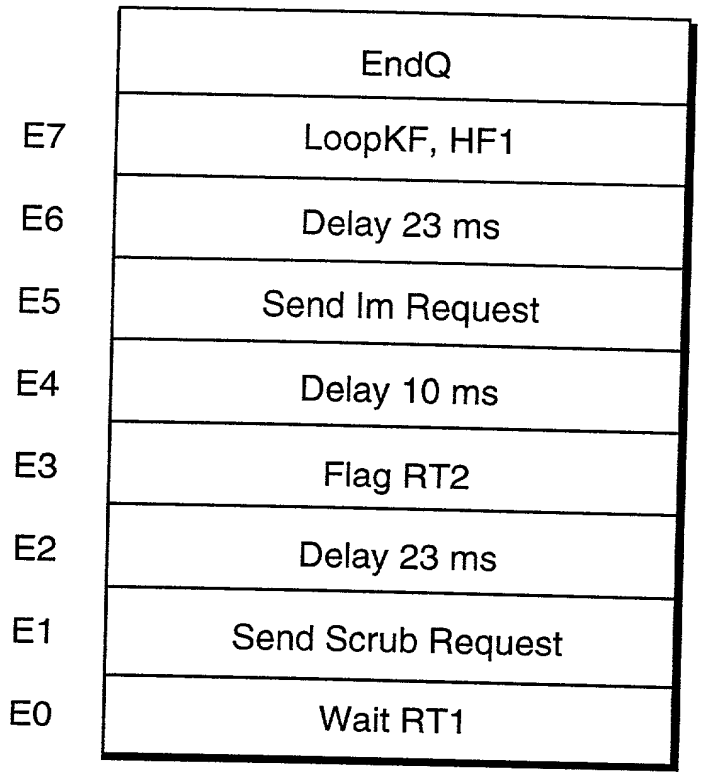

EndQ
E7
LoopKF, HF1
E6
Delay 23 ms
E5
Send Im Request
E4
Delay 10 ms
E3
Flag RT2
E2
Delay 23 ms
E1
Send Scrub Request
E0
Wait RT1
704
EVENT QUEUE

fig. 62

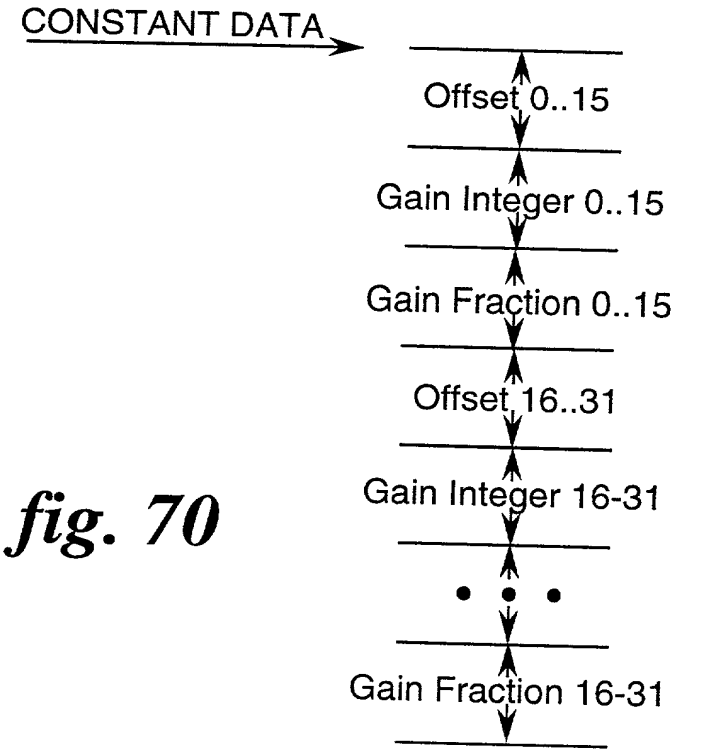

CONSTANT DATA
Offset 0..15
Gain Integer 0..15
Gain Fraction 0..15
Offset 16..31
Gain Integer 16-31
Gain Fraction 16-31
Constant Memory Format

fig. 70

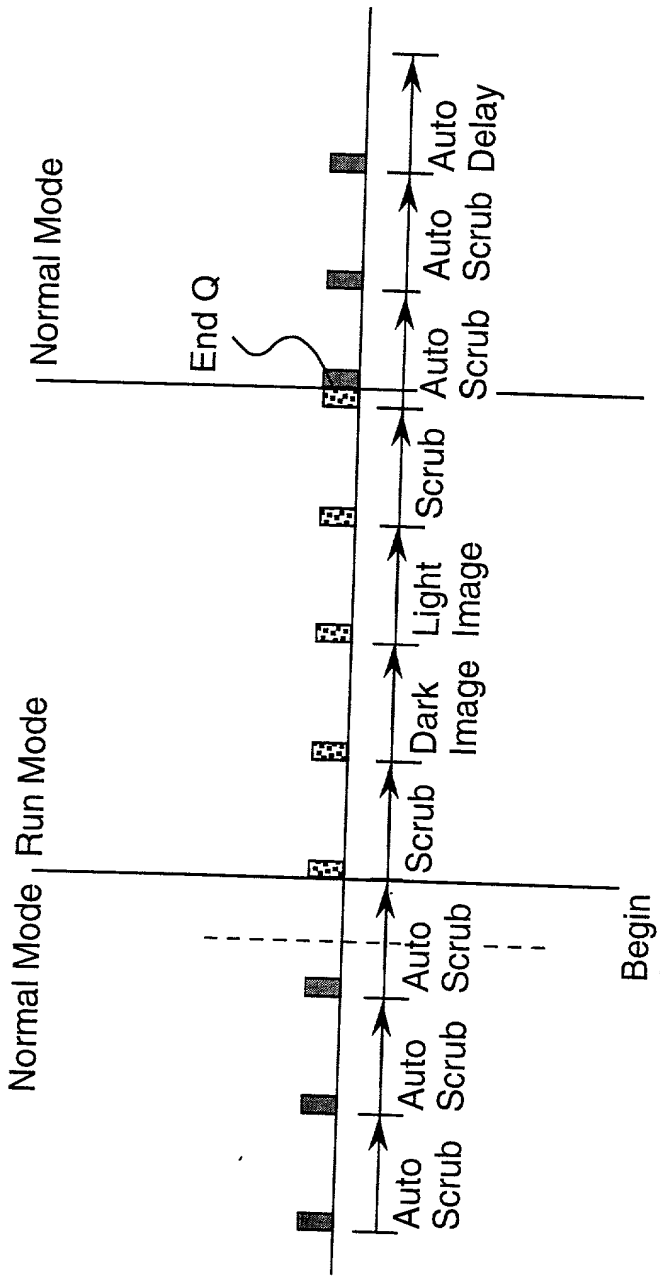

Normal Mode
Run Mode
Normal Mode
Begin Sequence Received
Auto Scrub
Auto Scrub
Auto Scrub
Scrub
Dark Image
Light Image
Scrub
End Q
Auto Scrub
Auto Scrub
Auto Delay

fig. 63

```
sequence_begin ( );
# define qv defaults:
%qv1 =('delay_qv' => 5000);
# call frame with qv's
frame_type1(NULL, \%qv1, 1);
  sequence_end ( );
```

fig. 64

```
sub frame
{
$QVf  = 'frame' ;
%qv = ('delay_qv' = > [10000]);
%qp = ( );
compile_init (@_,\%qp, \%qv, $QVf);
      Delay('Delay_qv1');
compile_finit ( );
 }
```

fig. 65


```
pDFN->DFNChangeQueueVariable
(
(char *) SymName,                    // variable name
(char *) sndBuf,                     // new value
BufSize                              // num bytes to write
  (ULONG *) & Debug                  // developer info
);
```

fig. 66

```
// load and run the event sequence
pDFNBeginSequenceNoMappingNoLog
      (snum,"d:\\HF.bin") ;
// assign data to be passed
sndBuf = 25000;
// change the queue variable
pDFN->DFNChange QueueVariable
(
  (char *) SymName,          // variable name
  (char *) sndBuf,           // new value
  (ULONG ) sizeof sndBuf     // num bytes to write
  (ULONG *) & debug          // developer info
);
```

fig. 67

```
sub frame_type1
{
 $HFfrm = 'frame_type1';
 %qv = ('delay_qv' = > [20000]);
 %qp = ( );
 $image_cmd  = [0x800000,0x0];
 compile_init (@_,\%qp, \%qv, $HFfrm);
    Send ( $image_cmd);
     Delay('delay_qv');
     LoopKF(2, 0xAAFF01);
    compile_finit( ) ;
}
```

fig. 68

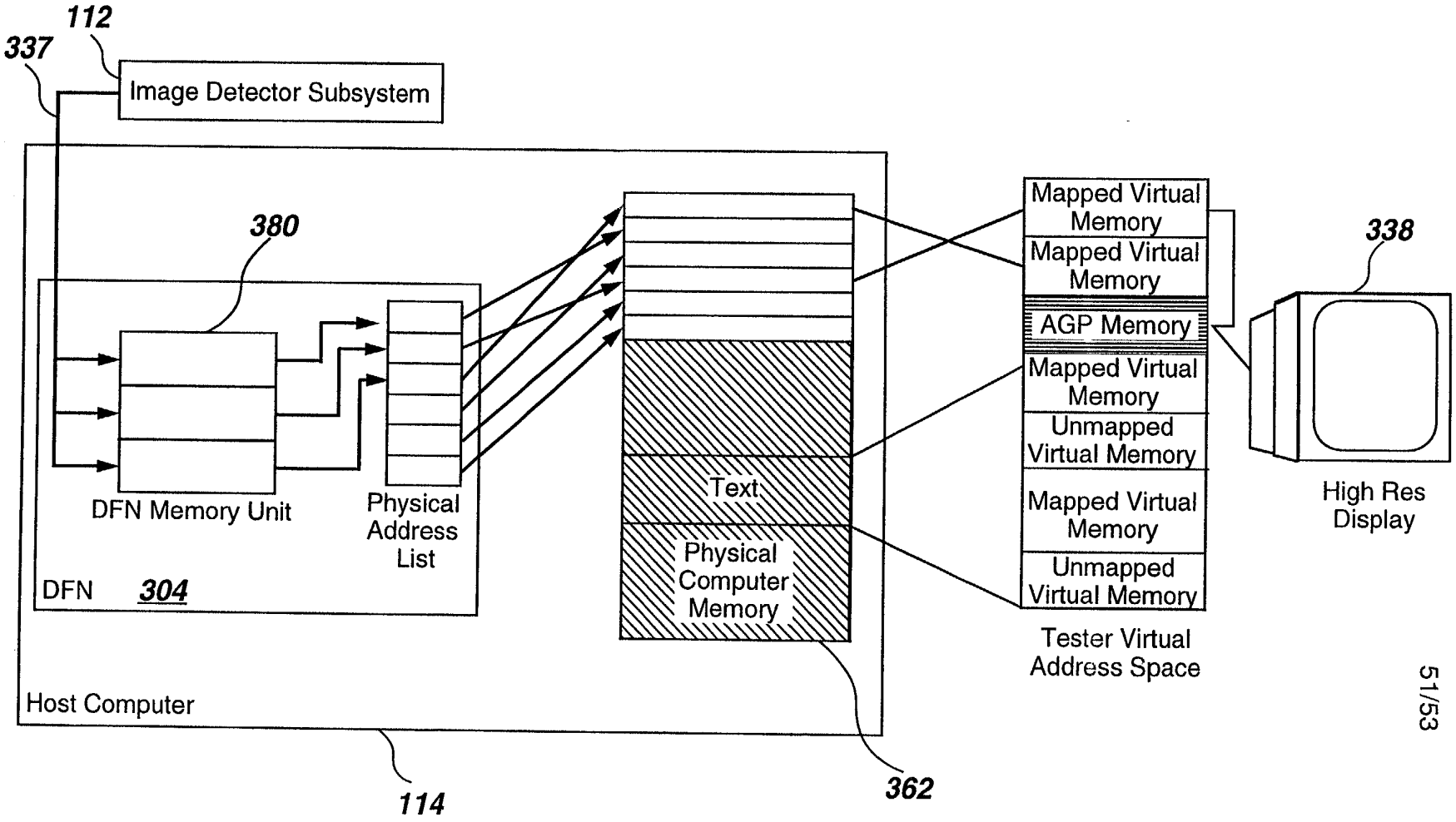

112
337
Image Detector Subsystem
380
DFN Memory Unit
Physical Address List
DFN 304
Host Computer
114
Text
Physical Computer Memory
362
Mapped Virtual Memory
Mapped Virtual Memory
AGP Memory
Mapped Virtual Memory
Unmapped Virtual Memory
Mapped Virtual Memory
Unmapped Virtual Memory
Tester Virtual Address Space
338
High Res Display

fig. 69

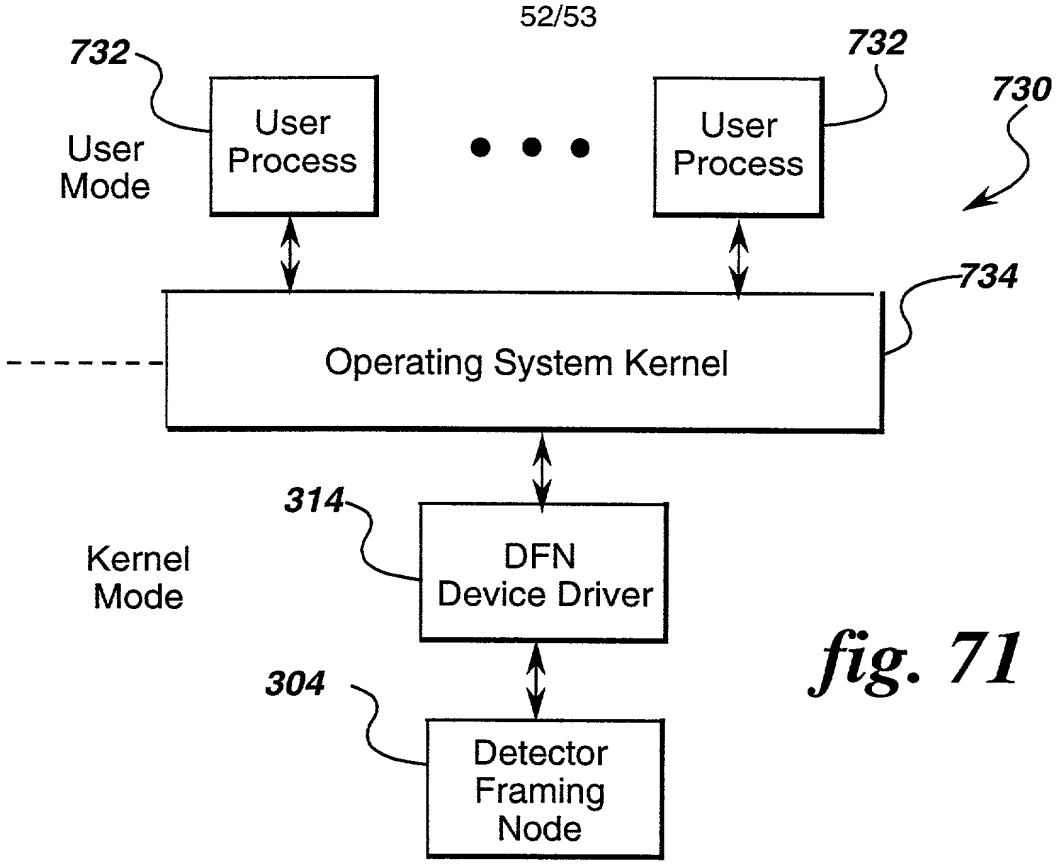

732
User Process
732
User Process
730
User Mode
734
Operating System Kernel
314
DFN Device Driver
Kernel Mode
304
Detector Framing Node

fig. 71

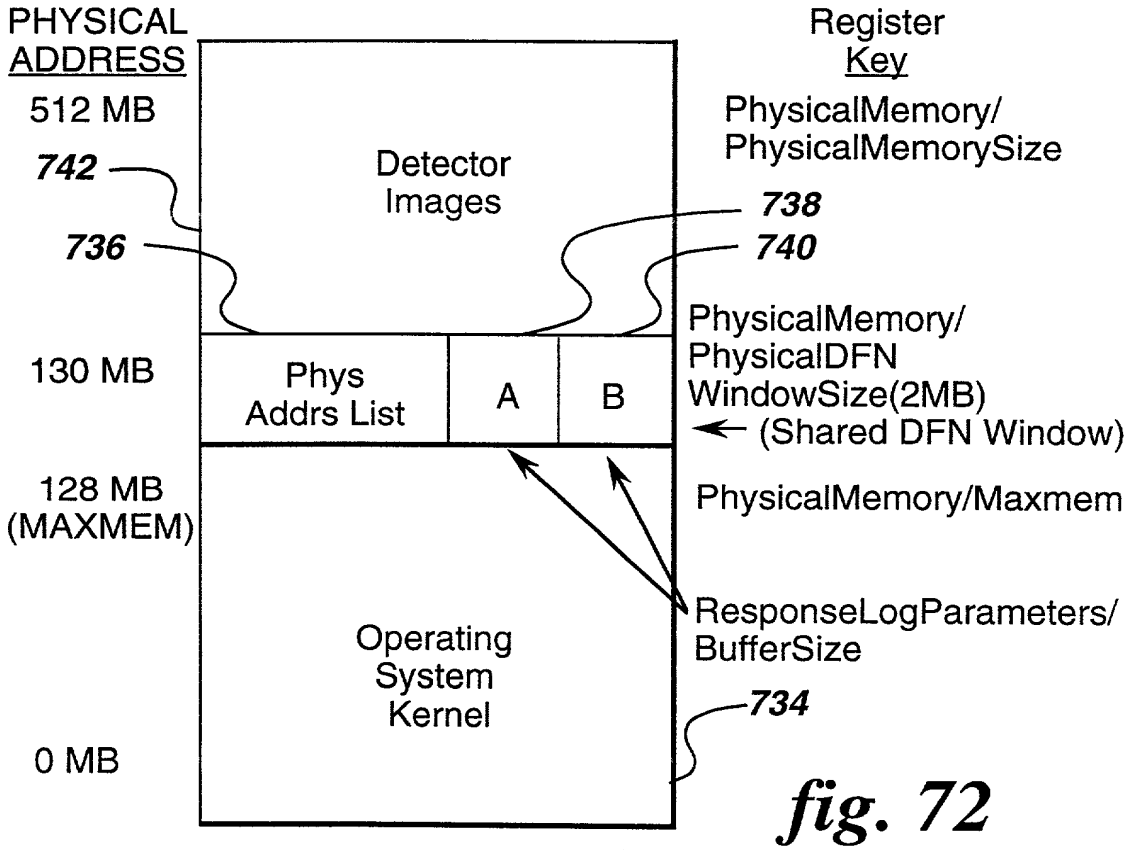

PHYSICAL ADDRESS
512 MB
742
736
Detector Images
Register Key
PhysicalMemory/ PhysicalMemorySize
738
740
PhysicalMemory/ PhysicalDFN WindowSize(2MB)
130 MB
Phys Addrs List
A
B
(Shared DFN Window)
128 MB (MAXMEM)
PhysicalMemory/Maxmem
ResponseLogParameters/ BufferSize
Operating System Kernel
734
0 MB

fig. 72

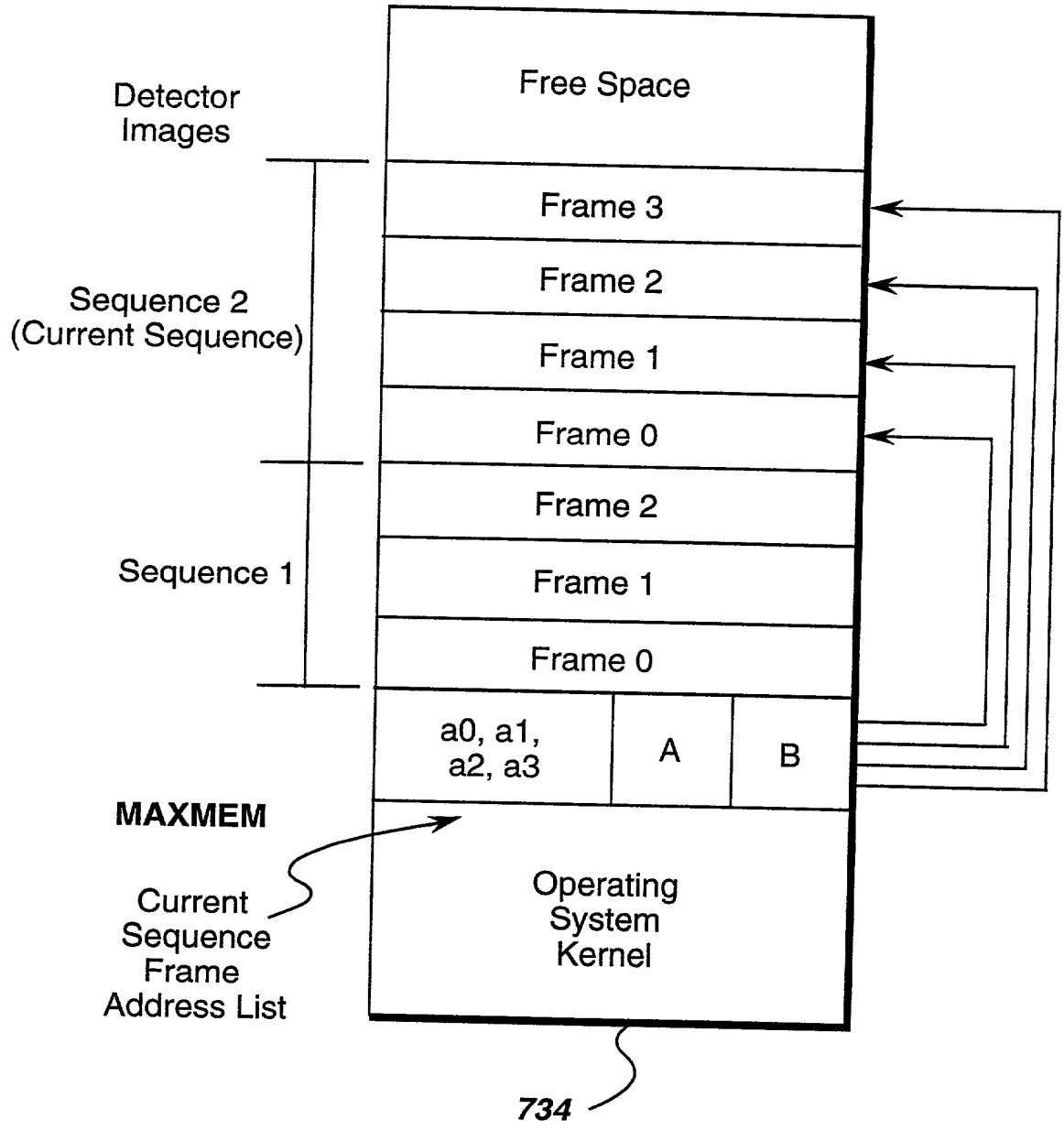

Free Space
Detector Images
Frame 3
Frame 2
Sequence 2 (Current Sequence)
Frame 1
Frame 0
Frame 2
Sequence 1
Frame 1
Frame 0
a0, a1, a2, a3
A
B
MAXMEM
Current Sequence Frame Address List
Operating System Kernel
734

fig. 73